

NTB45N06L, NTB45N06L

MOSFET – Power, N-Channel, Logic Level, D²PAK

45 A, 60 V, 28 mΩ

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- Higher Current Rating
- Lower $R_{DS(on)}$
- Lower $V_{DS(on)}$
- Lower Capacitances
- Lower Total Gate Charge
- Tighter V_{SD} Specification
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge
- AEC-Q101 Qualified and PPAP Capable – NTB45N06L
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

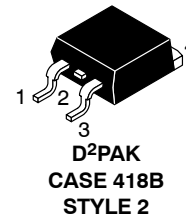
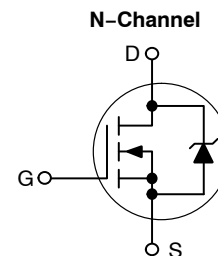


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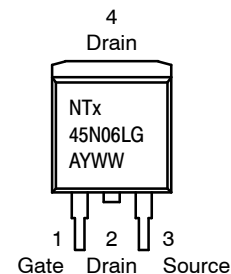
<http://onsemi.com>

45 AMPERES, 60 VOLTS

$R_{DS(on)} = 28\text{ m}\Omega$



MARKING DIAGRAM & PIN ASSIGNMENT1



NTx45N06L = Device Code
x = B or P
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NTB45N06L, NTB45N06L

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	60	Vdc
Drain-to-Gate Voltage (R _{GS} = 10 MΩ)	V _{DGR}	60	Vdc
Gate-to-Source Voltage - Continuous - Non-Repetitive (t _p ≤ 10 ms)	V _{GS} V _{GS}	± 15 ± 20	Vdc
Drain Current - Continuous @ T _A = 25°C - Continuous @ T _A = 100°C - Single Pulse (t _p ≤ 10 μs)	I _D I _D I _{DM}	45 30 150	Adc Adc Apk
Total Power Dissipation @ T _A = 25°C Derate above 25°C Total Power Dissipation @ T _A = 25°C (Note 1) Total Power Dissipation @ T _A = 25°C (Note 2)	P _D	125 0.83 3.2 2.4	W W/°C W W
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T _J = 25°C (V _{DD} = 50 Vdc, V _{GS} = 5.0 Vdc, L = 0.3 mH I _{L(pk)} = 40 A, V _{DS} = 60 Vdc, R _G = 25 Ω)	E _{AS}	240	mJ
Thermal Resistance - Junction-to-Case - Junction-to-Ambient (Note 1) - Junction-to-Ambient (Note 2)	R _{θJC} R _{θJA} R _{θJA}	1.2 46.8 63.2	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8 in from case for 10 seconds	T _L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 1" pad size, (Cu Area 1.127 in²).
2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in²).

ORDERING INFORMATION

Device	Package	Shipping†
NTB45N06LG	D ² PAK (Pb-Free)	50 Units / Rail
NTB45N06LT4G	D ² PAK (Pb-Free)	800 / Tape & Reel
NTBV45N06LT4G	D ² PAK (Pb-Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	60 –	67 67.2	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS} = ±15 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	±100	nAdc

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage (Note 4) (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 –	1.8 4.7	2.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 4) (V _{GS} = 5.0 Vdc, I _D = 22.5 Adc)	R _{DS(on)}	–	23	28	mΩ
Static Drain-to-Source On-Voltage (Note 4) (V _{GS} = 5.0 Vdc, I _D = 45 Adc) (V _{GS} = 5.0 Vdc, I _D = 22.5 Adc, T _J = 150°C)	V _{DS(on)}	– –	1.03 0.93	1.51 –	Vdc
Forward Transconductance (Note 4) (V _{DS} = 8.0 Vdc, I _D = 12 Adc)	g _{FS}	–	22.8	–	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	–	1212	1700	pF
Output Capacitance		C _{oss}	–	352	480	
Transfer Capacitance		C _{rss}	–	90	180	

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	(V _{DD} = 30 Vdc, I _D = 45 Adc, V _{GS} = 5.0 Vdc, R _G = 9.1 Ω) (Note 4)	t _{d(on)}	–	13	30	ns
Rise Time		t _r	–	341	680	
Turn-Off Delay Time		t _{d(off)}	–	36	75	
Fall Time		t _f	–	158	320	
Gate Charge	(V _{DS} = 48 Vdc, I _D = 45 Adc, V _{GS} = 5.0 Vdc) (Note 4)	Q _T	–	23	32	nC
	Q ₁	–	4.6	–		
	Q ₂	–	14.1	–		

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 45 Adc, V _{GS} = 0 Vdc) (Note 4) (I _S = 45 Adc, V _{GS} = 0 Vdc, T _J = 150°C)	V _{SD}	– –	1.01 0.92	1.15 –	Vdc
Reverse Recovery Time	(I _S = 45 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/μs) (Note 4)	t _{rr}	–	56	–	ns
		t _a	–	30	–	
		t _b	–	26	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.09	–	μC

3. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in²).

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

NTB45N06L, NTBV45N06L

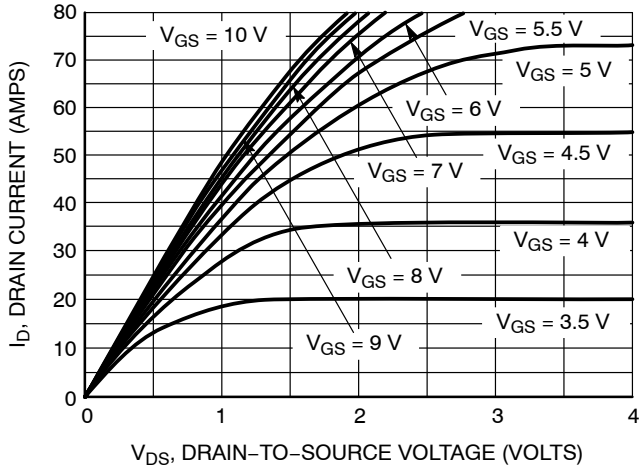


Figure 1. On-Region Characteristics

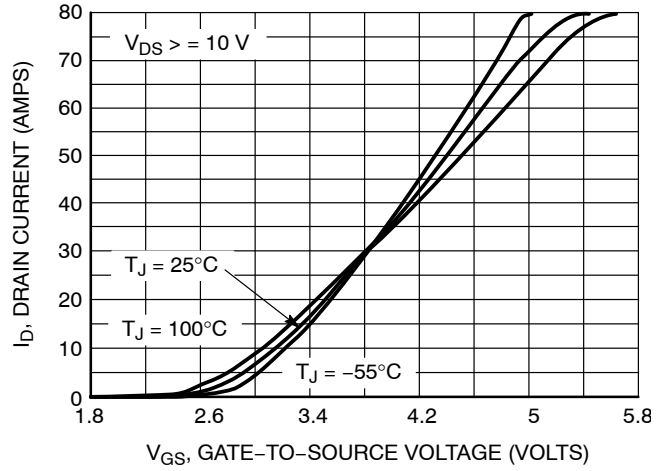


Figure 2. Transfer Characteristics

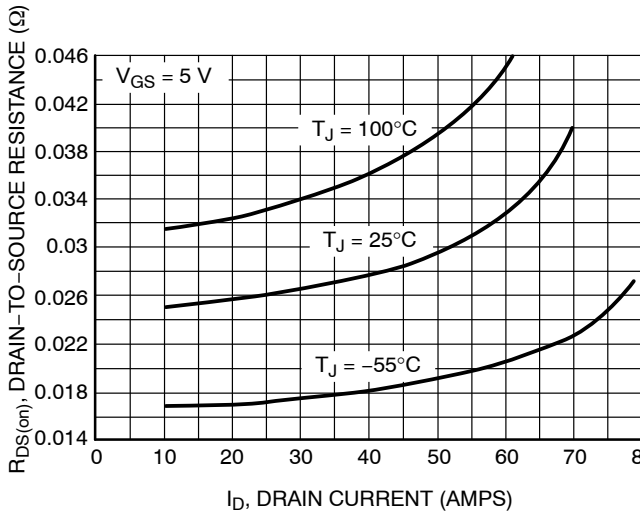


Figure 3. On-Resistance vs. Gate-to-Source Voltage

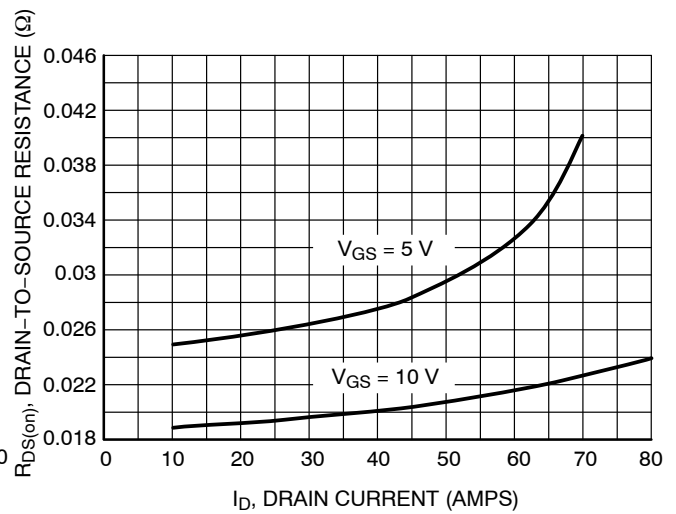


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

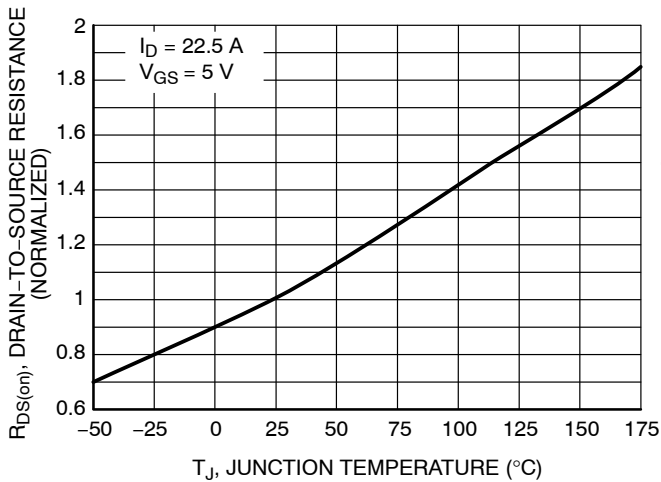


Figure 5. On-Resistance Variation with Temperature

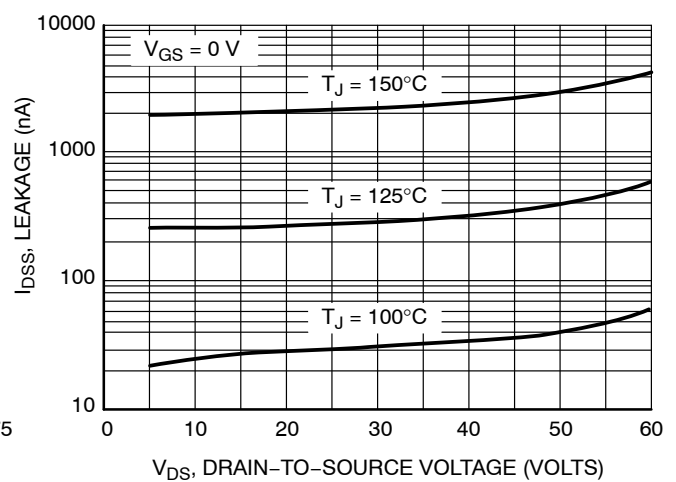


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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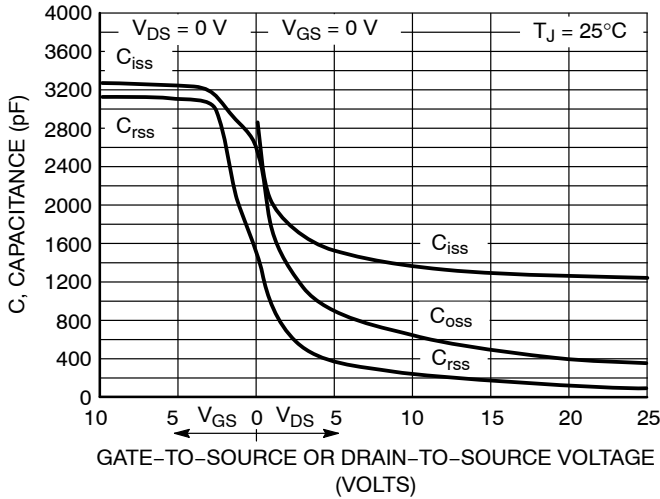


Figure 7. Capacitance Variation

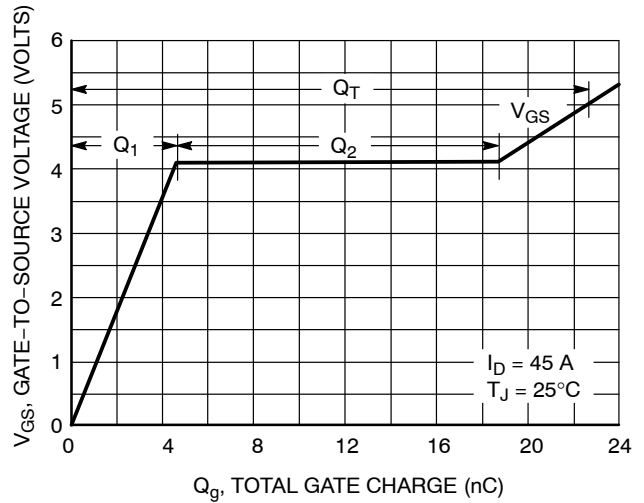


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

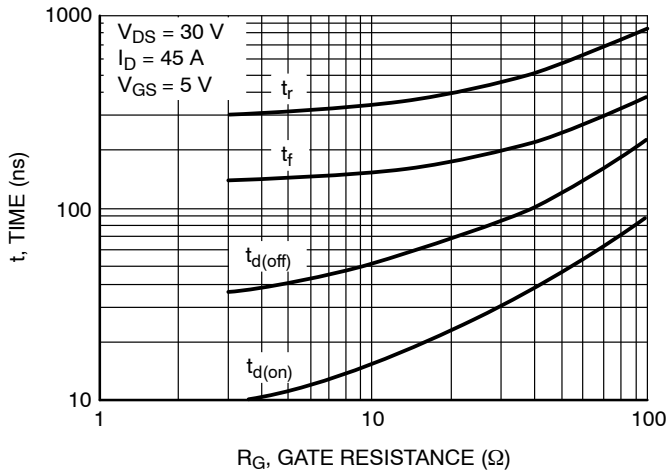


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

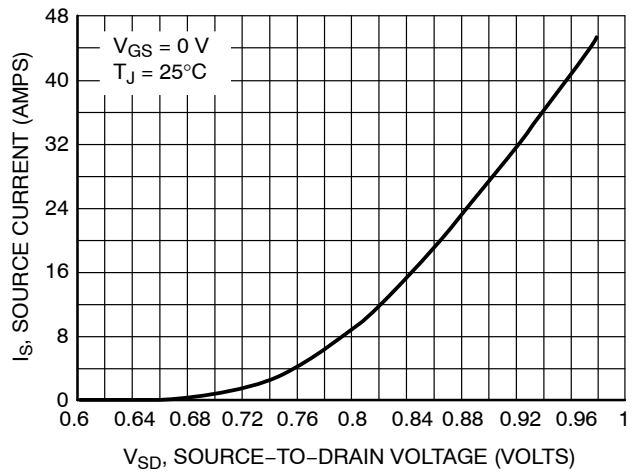


Figure 10. Diode Forward Voltage vs. Current

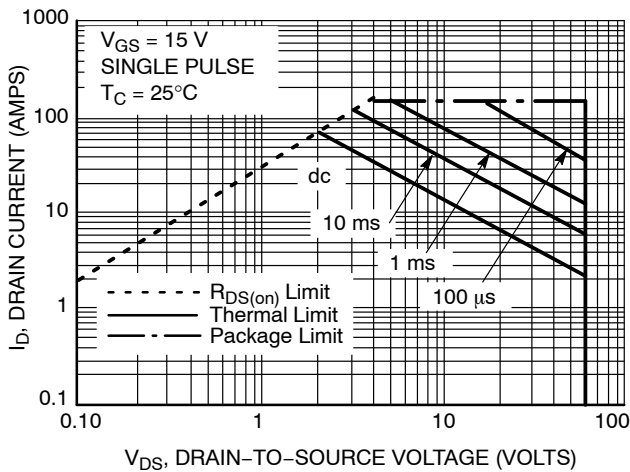


Figure 11. Maximum Rated Forward Biased Safe Operating Area

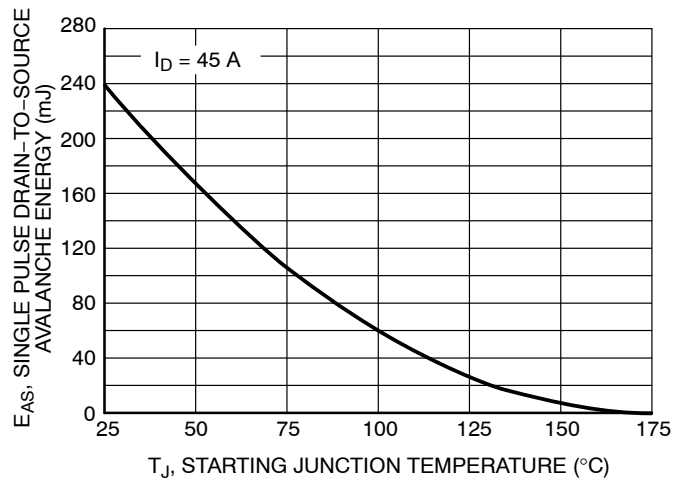


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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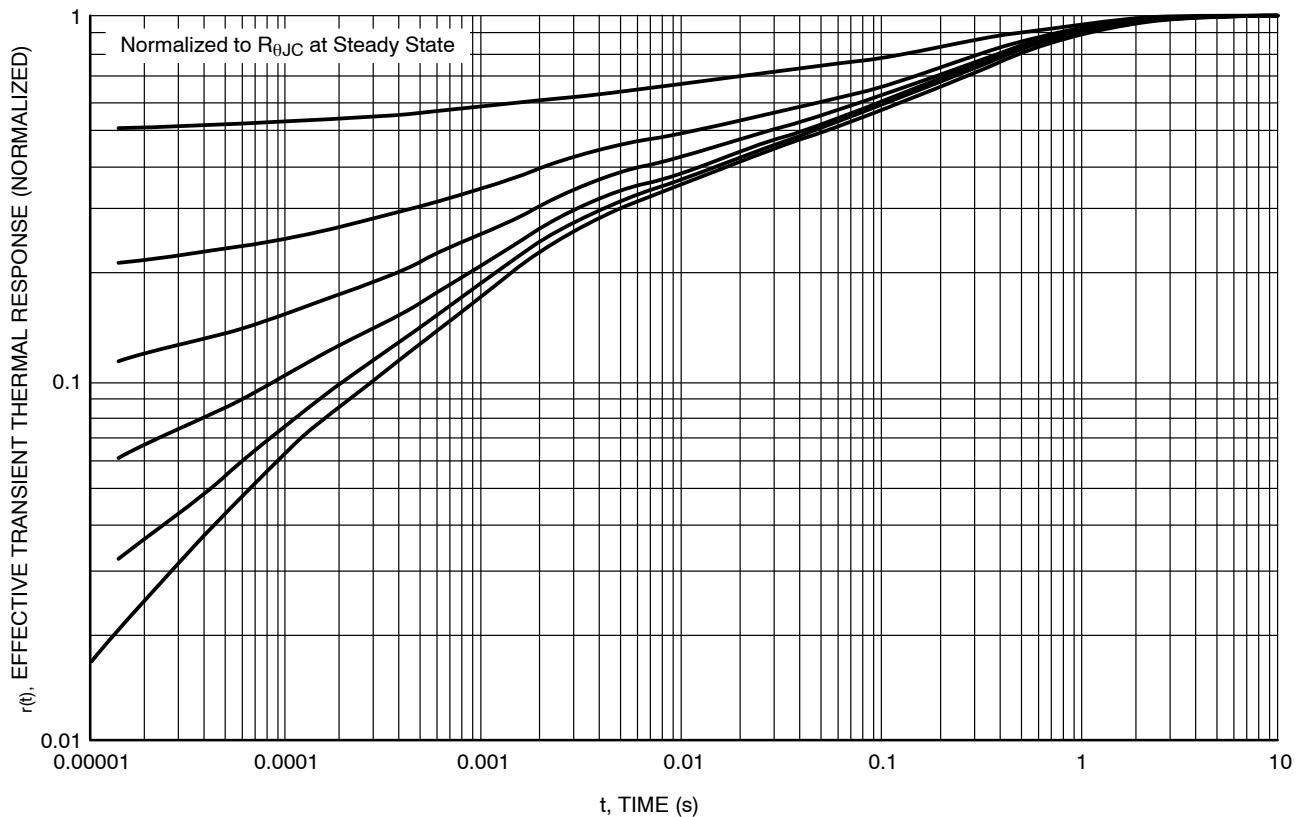


Figure 13. Thermal Response

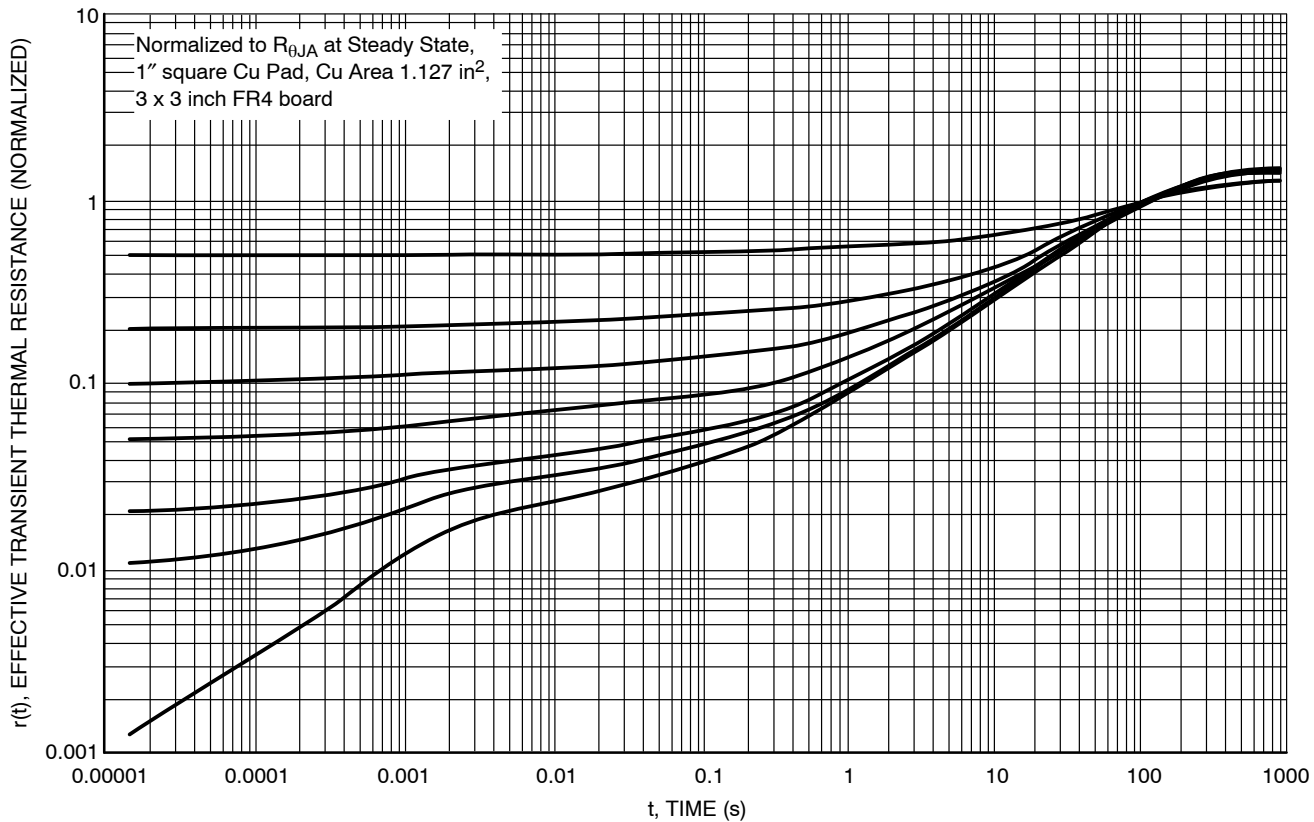


Figure 14. Thermal Response

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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D²PAK 3
CASE 418B-04
ISSUE L

DATE 17 FEB 2015

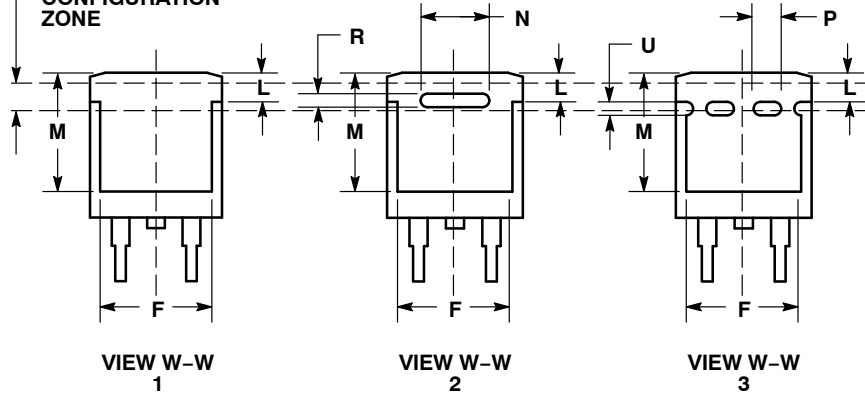
SCALE 1:1



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: INCH.
 - 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

VARIABLE CONFIGURATION ZONE



- | | | | | | |
|---|--|--|---|--|---|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE | STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE | STYLE 6:
PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE |
|---|--|--|---|--|---|

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D²PAK 3
CASE 418B-04
ISSUE L

DATE 17 FEB 2015

**GENERIC
MARKING DIAGRAM***



- xx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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