

# MOSFET - Power, N-Channel, DPAK

#### 14 A, 25 V

## NTD14N03R, NVD14N03R

#### **Features**

- Planar HD3e Process for Fast Switching Performance
- Low R<sub>DS(on)</sub> to Minimize Conduction Loss
- Low C<sub>iss</sub> to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters
- NVD and SVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

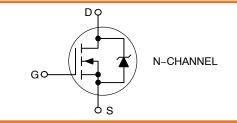
#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	25	Vdc
Gate-to-Source Voltage - Continuous	V <sub>GS</sub>	±20	Vdc
Thermal Resistance – Junction–to–Case Total Power Dissipation @ $T_A$ = 25°C Drain Current – Continuous @ $T_A$ = 25°C, Chip – Continuous @ $T_A$ = 25°C, Limited by Package – Single Pulse (tp $\leq$ 10 $\mu$ s)	R <sub>θJC</sub> P <sub>D</sub> I <sub>D</sub> I <sub>D</sub>	6.0 20.8 14 11.4 28	°C/W W A A A
Thermal Resistance, Junction-to-Ambient (Note 1) Total Power Dissipation @ T <sub>A</sub> = 25°C Drain Current - Continuous @ T <sub>A</sub> = 25°C	R <sub>θJA</sub> P <sub>D</sub> I <sub>D</sub>	80 1.56 3.1	°C/W W A
Thermal Resistance, Junction-to-Ambient (Note 2) Total Power Dissipation @ T <sub>A</sub> = 25°C Drain Current - Continuous @ T <sub>A</sub> = 25°C	R <sub>θJA</sub> P <sub>D</sub> I <sub>D</sub>	120 1.04 2.5	°C/W W A
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T <sub>L</sub>	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. When surface mounted to an FR4 board using 0.5 sq. in pad size.
- When surface mounted to an FR4 board using minimum recommended pad size.

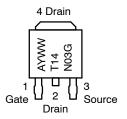
## 14 AMPERES, 25 VOLTS $R_{DS(on)} = 70.4 \text{ m}\Omega \text{ (Typ)}$





DPAK
CASE 369C
(Surface Mount)
STYLE 2

## MARKING DIAGRAM & PIN ASSIGNMENTS



A = Assembly Location\* Y = Year

WW = Work Week
14N03 = Device Code
G = Pb-Free Package

\* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

#### **ORDERING INFORMATION**

See detailed ordering and shipping information on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

#### **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Chara	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS			1			1
Drain-to-Source Breakdown Voltag (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V(br) <sub>DSS</sub>	25 -	28 -	- -	Vdc mV/°C	
Zero Gate Voltage Drain Current $(V_{DS} = 20 \text{ Vdc}, V_{GS} = 0 \text{ Vdc})$ $(V_{DS} = 20 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}, T_J = 150^{\circ}\text{C})$		I <sub>DSS</sub>	_ _	- -	1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	±100	nAdc	
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) $(V_{DS} = V_{GS}, I_D = 250 \mu Adc)$ Threshold Temperature Coefficient (	V <sub>GS(th)</sub>	1.0	1.5 -	2.0 -	Vdc mV/°C	
Static Drain-to-Source On-Resista $(V_{GS} = 4.5 \text{ Vdc}, I_D = 5 \text{ Adc})$ $(V_{GS} = 10 \text{ Vdc}, I_D = 5 \text{ Adc})$	R <sub>DS(on)</sub>	- -	117 70.4	130 95	mΩ	
Forward Transconductance (Note 3) (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 5 Adc)	9FS	_	7.0	i	Mhos	
DYNAMIC CHARACTERISTICS						
Input Capacitance		C <sub>iss</sub>	_	115	-	pF
Output Capacitance	$(V_{DS} = 20 \text{ Vdc}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz})$	C <sub>oss</sub>	_	62	_	
Transfer Capacitance		C <sub>rss</sub>	_	33	-	
SWITCHING CHARACTERISTICS	(Note 4)					
Turn-On Delay Time		t <sub>d(on)</sub>	_	3.8	i	ns
Rise Time	(V <sub>GS</sub> = 10 Vdc, V <sub>DD</sub> = 10 Vdc,	t <sub>r</sub>	_	27	i	
Turn-Off Delay Time	$I_D = 5 \text{ Adc}, R_G = 3 \Omega$	t <sub>d(off)</sub>	_	9.6	i	
Fall Time		t <sub>f</sub>	_	2.0	-	
Gate Charge		$Q_{T}$	_	1.8	i	nC
	$(V_{GS} = 5 \text{ Vdc}, I_D = 5 \text{ Adc}, V_{DS} = 10 \text{ Vdc}) \text{ (Note 3)}$	Q <sub>1</sub>	_	0.8	-	
	, , ,	$Q_2$	-	0.7	-	
SOURCE-DRAIN DIODE CHARAC	TERISTICS					
Forward On-Voltage	$(I_S = 5 \text{ Adc}, V_{GS} = 0 \text{ Vdc}) \text{ (Note 3)}$ $(I_S = 5 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 125^{\circ}\text{C})$	V <sub>SD</sub>	- -	0.93 0.82	1.2 -	V <sub>dc</sub>
Reverse Recovery Time		t <sub>rr</sub>	-	6.6	-	ns
	(I <sub>S</sub> = 5 Adc, V <sub>GS</sub> = 0 Vdc,	ta	-	4.75	-	
	dl <sub>S</sub> /dt = 100 A/μs) (Note 3)	t <sub>b</sub>	-	1.88	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	_	0.002	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

#### **TYPICAL CHARACTERISTICS**

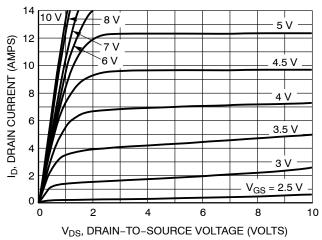


Figure 1. On-Region Characteristics

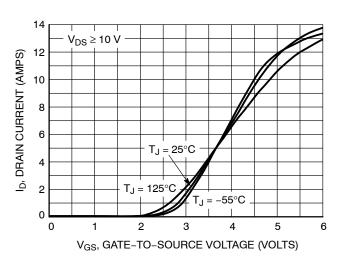


Figure 2. Transfer Characteristics

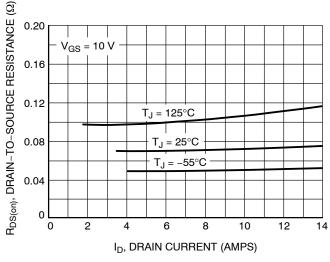


Figure 3. On-Resistance versus Drain Current and Temperature

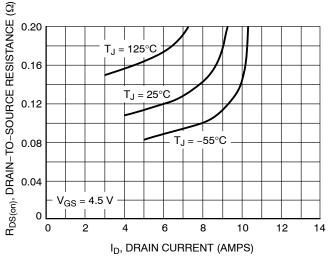


Figure 4. On-Resistance versus Drain Current and Temperature

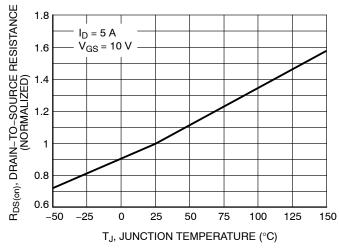


Figure 5. On–Resistance Variation with Temperature

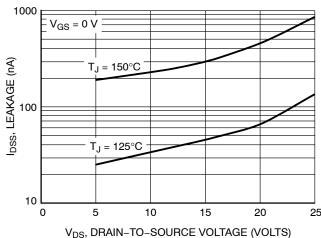


Figure 6. Drain-to-Source Leakage Current versus Voltage

#### **TYPICAL CHARACTERISTICS**

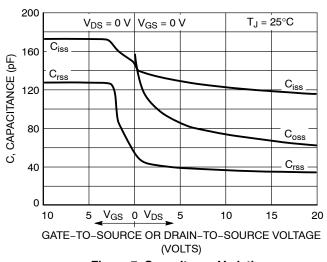


Figure 7. Capacitance Variation

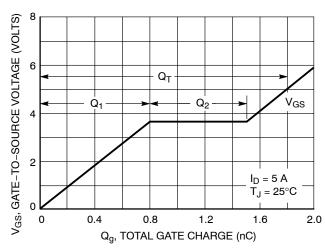


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

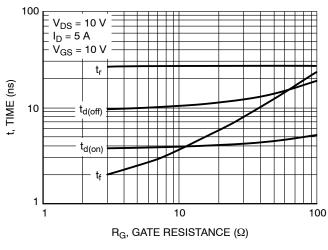


Figure 9. Resistive Switching Time Variation versus Gate Resistance

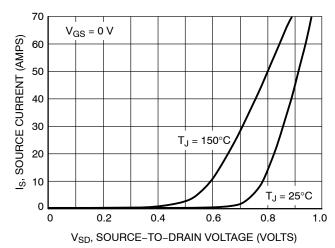


Figure 10. Diode Forward Voltage versus Current

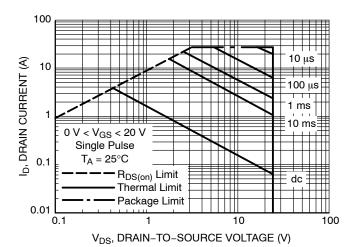


Figure 11. Maximum Rated Forward Biased Safe Operating Area

#### **TYPICAL CHARACTERISTICS**

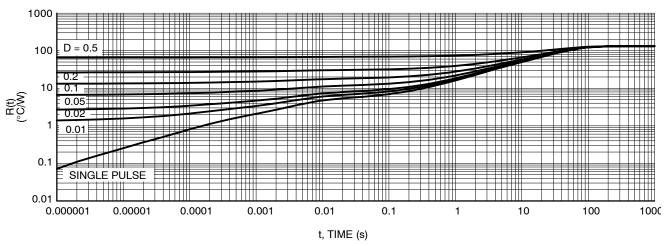


Figure 12. Thermal Response

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NTD14N03RT4G	DPAK (Pb-Free)	2500 / Tape & Reel

#### **DISCONTINUED** (Note 5)

NVD14N03RT4G*	DPAK (Pb-Free)	2500 / Tape & Reel
SVD14N03RT4G*	DPAK (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

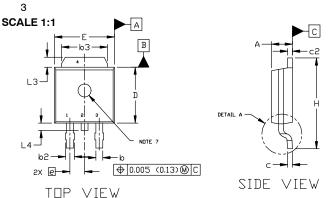
<sup>\*</sup>NVD and SVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

<sup>5.</sup> **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on <a href="https://www.onsemi.com">www.onsemi.com</a>.

### **DPAK (SINGLE GAUGE)**

CASE 369C **ISSUE G** 

**DATE 31 MAY 2023** 

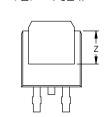


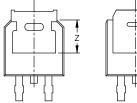


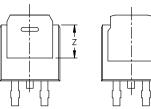
- DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994. CONTROLLING DIMENSION: INCHES
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS 63,
- L3. AND Z. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH,
  PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR
  GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE DUTERMOST EXTREMES OF THE PLASTIC BODY.

  DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
- OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
Α	0.086	0.094	2.18	2.38	
A1	0.000	0.005	0.00	0.13	
b	0.025	0.035	0.63	0.89	
b2	0.028	0.045	0.72	1.14	
b3	0.180	0.215	4.57	5.46	
С	0.018	0.024	0.46	0.61	
c2	0.018	0.024	0.46	0.61	
D	0.235	0.245	5.97	6.22	
E	0.250	0.265	6.35	6.73	
е	0.090 BSC		2.29 BSC		
Н	0.370	0.410	9.40	10.41	
L	0.055	0.070	1.40	1.78	
L1	0.114 REF		2.90	REF	
L2	0.020 BSC		0.51	0.51 BSC	
L3	0.035	0.050	0.89	1.27	
L4		0.040		1.01	
Z	0.155		3.93		





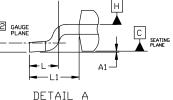


BOTTOM VIEW

5.80

BOTTOM VIEW ALTERNATE

CONSTRUCTIONS [0.228] 6.20 L2 GAUGE PLANE [0.244] 2.58 3.00 [0.102] [0.118] 1.60 [0.063] 6.17



STYLE 5: PIN 1. GATE

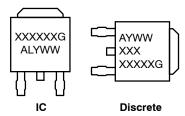
2. ANODE

3 CATHODE

ANODE

CW ROTATED 90°

#### **GENERIC MARKING DIAGRAM\***



= Device Code
= Assembly Location
= Wafer Lot
= Year
= Work Week
= Pb-Free Package

RECOMMENDED MOUNTING FOOTPRINT\* \*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DUWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

[0.243]

STYLE 1: PIN 1. BASE STYLE 2: PIN 1. GATE STYLE 3: PIN 1. ANODE STYLE 4: PIN 1. CATHODE 2. COLLECTOR 2. DRAIN 2. CATHODE 2. ANODE 3 SOURCE 3 FMITTER 3 ANODE 3 GATE

COLLECTOR 4. DRAIN 4. CATHODE 4. ANODE STYLE 6: STYLE 7: PIN 1. GATE 2. COLLECTOR STYLE 8: STYLE 9: PIN 1. MT1 2. MT2

STYLE 10: PIN 1. N/C 2. CATHODE 3. ANODE PIN 1. ANODE 2. CATHODE PIN 1. CATHODE 2. ANODE 3 CATHODE 3 FMITTER 3 RESISTOR ADJUST 4. COLLECTOR 4. CATHODE 4. ANODE CATHODE

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DPAK (SINGLE GAUGE)		PAGE 1 OF 1	

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3 GATE

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