

# MOSFET - Power, N-Channel, DPAK

## 20 A, 30 V

### NTD20N03L27, NVD20N03L27

This logic level vertical power MOSFET is a general purpose part that provides the “best of design” available today in a low cost power package. Avalanche energy issues make this part an ideal design in. The drain-to-source diode has a ideal fast but soft recovery.

#### Features

- Ultra-Low  $R_{DS(on)}$ , Single Base, Advanced Technology
- SPICE Parameters Available
- Diode is Characterized for use in Bridge Circuits
- $I_{DSS}$  and  $V_{DS(on)}$  Specified at Elevated Temperatures
- High Avalanche Energy Specified
- ESD JEDAC rated HBM Class 1, MM Class A, CDM Class 0
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### Typical Applications

- Power Supplies
- Inductive Loads
- PWM Motor Controls
- Replaces MTD20N03L in many Applications

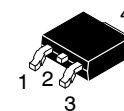
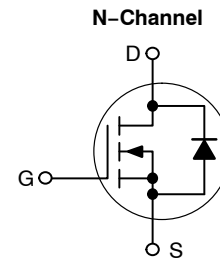
#### MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	30	Vdc
Drain-to-Gate Voltage (R <sub>GS</sub> = 1.0 MΩ)	$V_{DGR}$	30	Vdc
Gate-to-Source Voltage – Continuous – Non-Repetitive (t <sub>p</sub> ≤ 10 ms)	$V_{GS}$ $V_{GS}$	±20 ±24	Vdc
Drain Current – Continuous @ T <sub>A</sub> = 25°C – Continuous @ T <sub>A</sub> = 100°C – Single Pulse (t <sub>p</sub> ≤ 10 μs)	$I_D$ $I_D$ $I_{DM}$	20 16 60	Adc Apk
Total Power Dissipation @ T <sub>A</sub> = 25°C Derate above 25°C	$P_D$	74 0.6	W W/°CW
Total Power Dissipation @ T <sub>C</sub> = 25°C (Note 1)		1.75	
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T <sub>J</sub> = 25°C (V <sub>DD</sub> = 30 Vdc, V <sub>GS</sub> = 5 Vdc, L = 1.0 mH, I <sub>L(pk)</sub> = 24 A, V <sub>DS</sub> = 34 Vdc)	$E_{AS}$	288	mJ
Thermal Resistance – Junction-to-Case – Junction-to-Ambient – Junction-to-Ambient (Note 1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.67 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T <sub>L</sub>	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

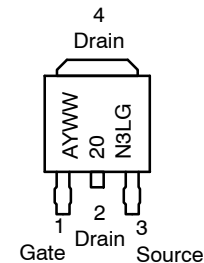
1. When surface mounted to an FR4 board using the minimum recommended pad size and repetitive rating; pulse width limited by maximum junction temperature.

20 A, 30 V,  $R_{DS(on)} = 27 \text{ m}\Omega$



DPAK  
CASE 369C  
STYLE 2

#### MARKING DIAGRAM & PIN ASSIGNMENTS



- A = Assembly Location\*
- 20N3L = Device Code
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# NTD20N03L27, NVD20N03L27

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-to-Source Breakdown Voltage (Note 2) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	30	–	–	Vdc
		–	43	–	mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 30 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 30 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	–	–	10	μAdc
		–	–	100	
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	–	–	±100	nAdc

## ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage (Note 2) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0	1.6	2.0	Vdc
		–	5.0	–	mV/°C
Static Drain-to-Source On-Resistance (Note 2) (V <sub>GS</sub> = 4.0 Vdc, I <sub>D</sub> = 10 Adc) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 10 Adc)	R <sub>DS(on)</sub>	–	28	31	mΩ
		–	23	27	
Static Drain-to-Source On-Voltage (Note 2) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 20 Adc) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 10 Adc, T <sub>J</sub> = 150°C)	V <sub>DS(on)</sub>	–	0.48	0.54	Vdc
		–	0.40	–	
Forward Transconductance (Note 2) (V <sub>DS</sub> = 5.0 Vdc, I <sub>D</sub> = 10 Adc)	g <sub>FS</sub>	–	21	–	mhos

## DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>ISS</sub>	–	1005	1260	pF
Output Capacitance		C <sub>OSS</sub>	–	271	420	
Transfer Capacitance		C <sub>RSS</sub>	–	87	112	

## SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	(V <sub>DD</sub> = 20 Vdc, I <sub>D</sub> = 20 Adc, V <sub>GS</sub> = 5.0 Vdc, R <sub>G</sub> = 9.1 Ω) (Note 2)	t <sub>d(on)</sub>	–	17	25	ns
Rise Time		t <sub>r</sub>	–	137	160	
Turn-Off Delay Time		t <sub>d(off)</sub>	–	38	45	
Fall Time		t <sub>f</sub>	–	31	40	
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 15 Adc, V <sub>GS</sub> = 10 Vdc) (Note 2)	Q <sub>T</sub>	–	13.8	18.9	nC
		Q <sub>1</sub>	–	2.8	–	
		Q <sub>2</sub>	–	6.6	–	

## SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = 20 Adc, V <sub>GS</sub> = 0 Vdc) (Note 2) (I <sub>S</sub> = 20 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	–	1.0	1.15	Vdc
			–	0.9	–	
Reverse Recovery Time	(I <sub>S</sub> = 15 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs) (Note 2)	t <sub>rr</sub>	–	23	–	ns
		t <sub>a</sub>	–	13	–	
		t <sub>b</sub>	–	10	–	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	–	0.017	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3. Switching characteristics are independent of operating junction temperature.

## ORDERING INFORMATION

Device	Package	Shipping†
NTD20N03L27T4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD20N03L27T4G*	DPAK (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

TYPICAL CHARACTERISTICS

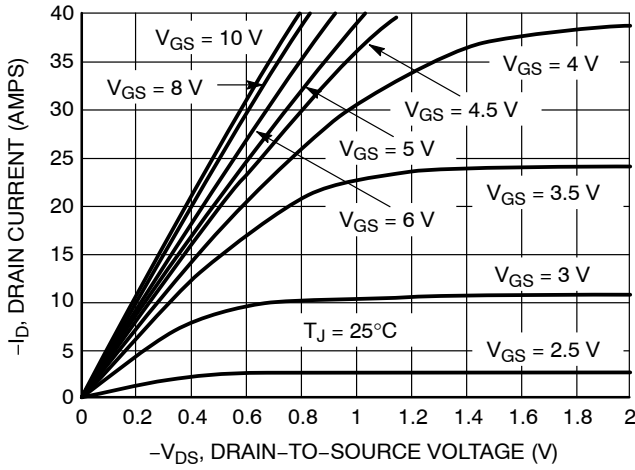


Figure 1. On-Region Characteristics

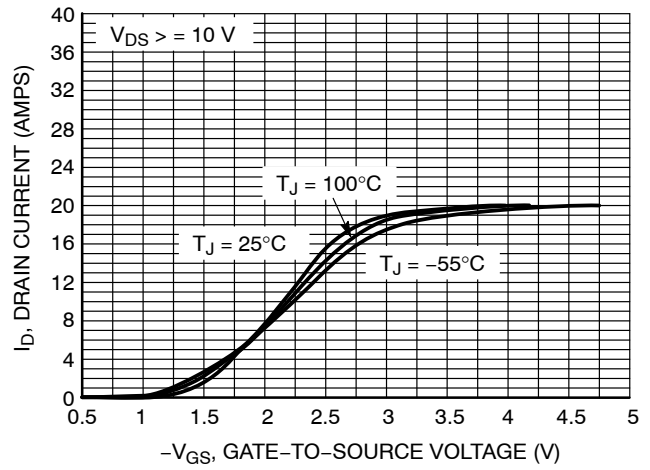


Figure 2. Transfer Characteristics

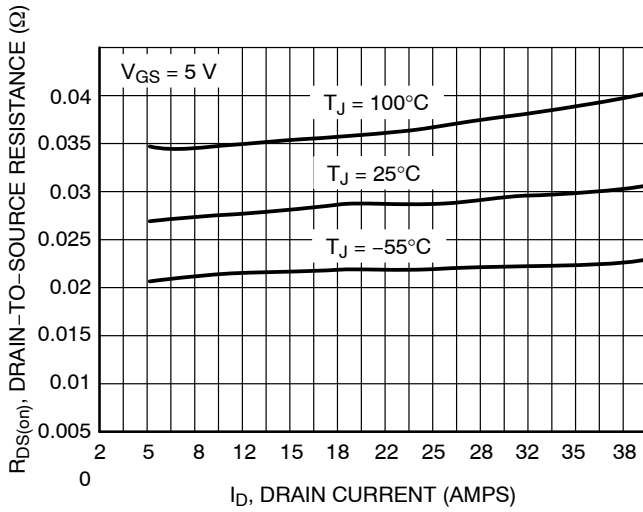


Figure 3. On-Resistance vs. Drain Current and Temperature

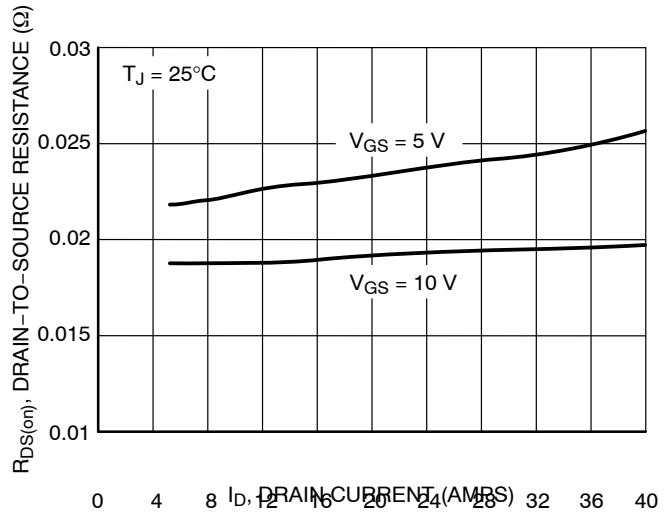


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

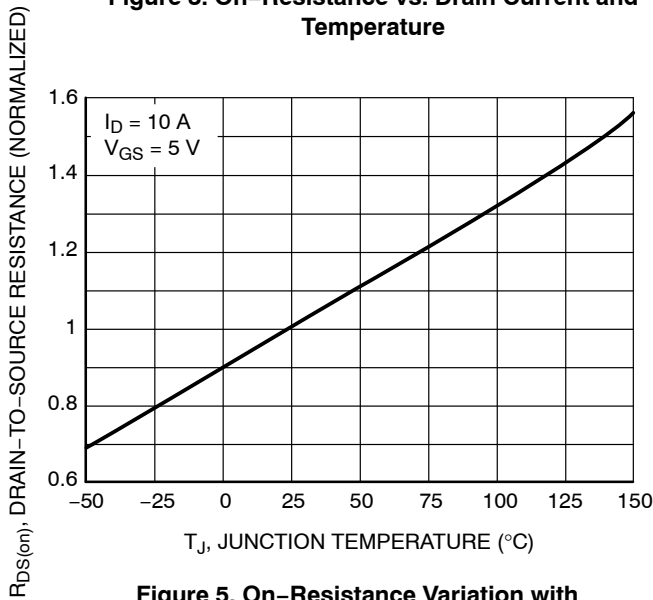


Figure 5. On-Resistance Variation with Temperature

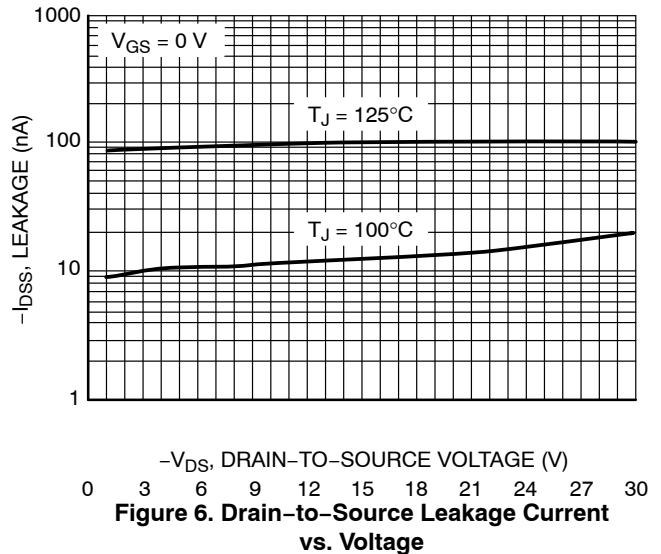


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

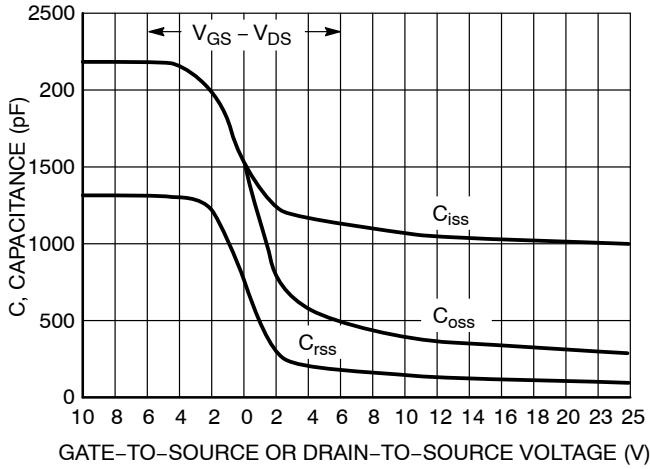


Figure 7. Capacitance Variation

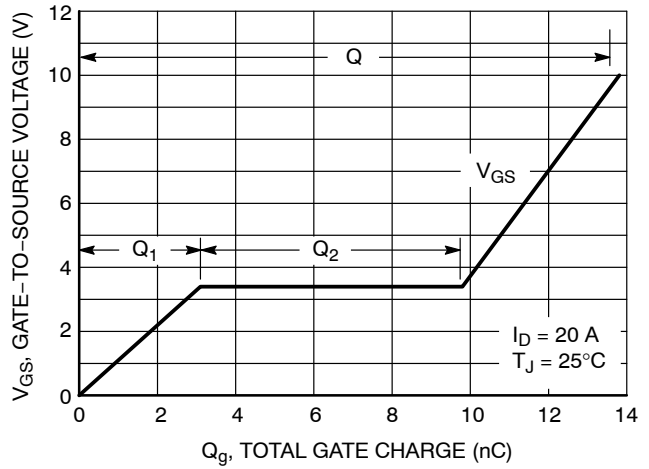


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

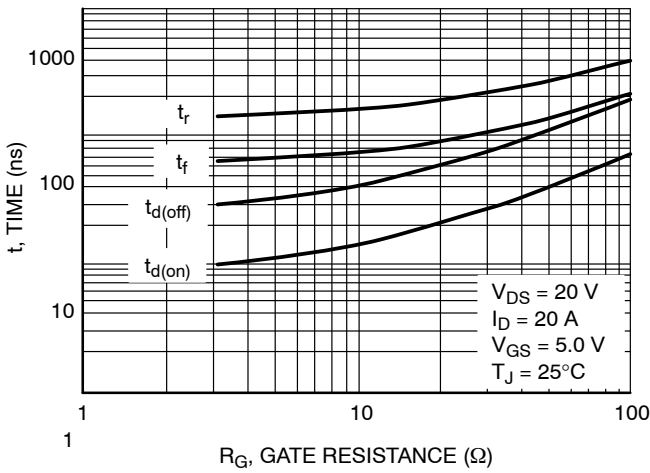


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

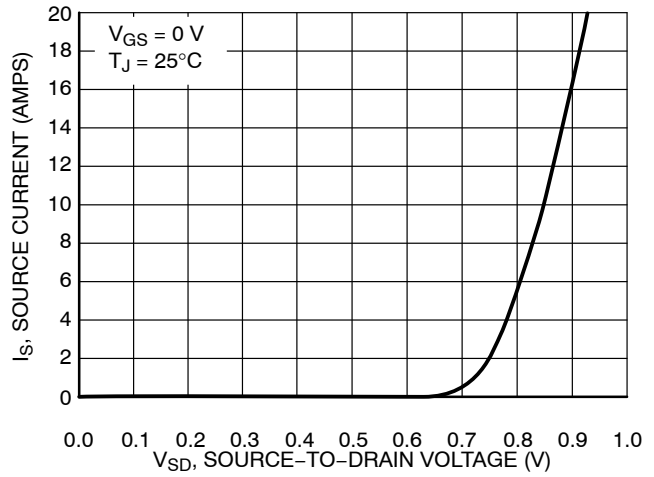


Figure 10. Diode Forward Voltage vs. Current

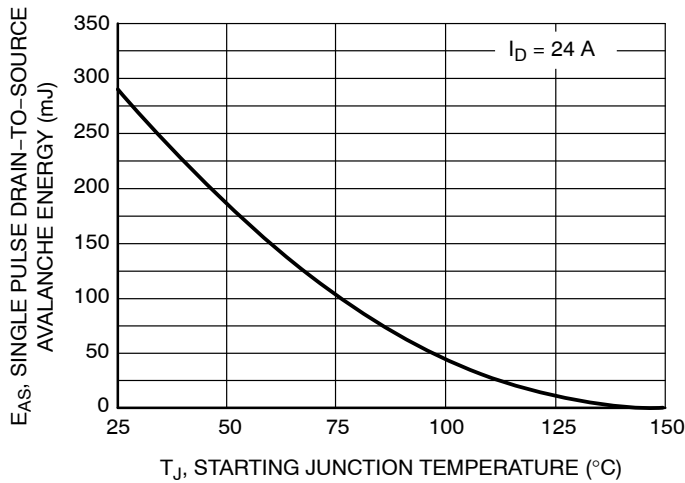


Figure 11. Maximum Avalanche Energy vs. Starting Junction Temperature

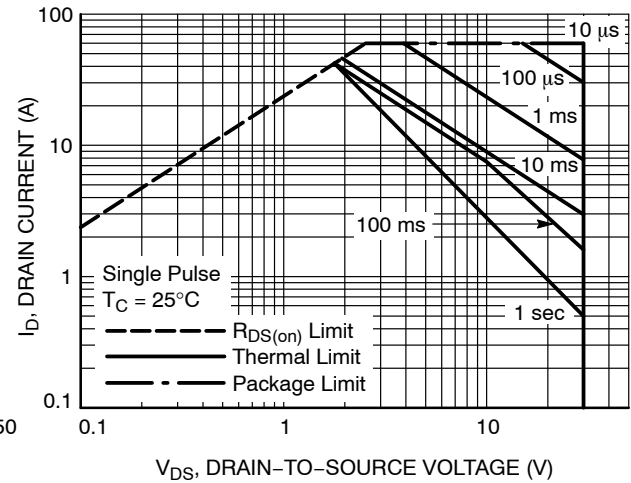


Figure 12. Safe Operating Area

# NTD20N03L27, NVD20N03L27

## TYPICAL CHARACTERISTICS

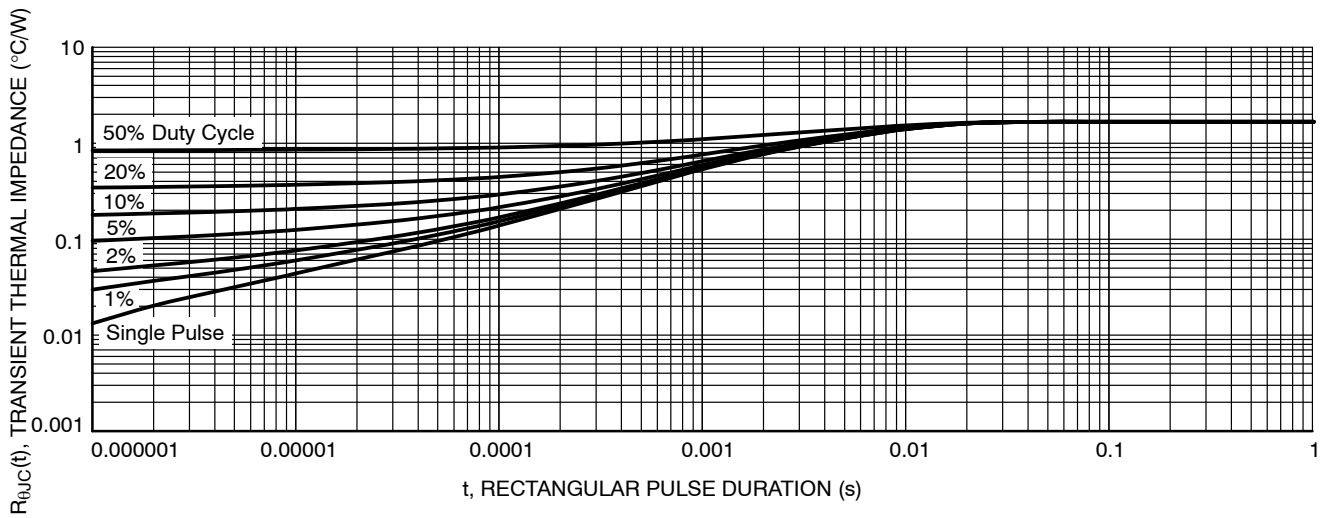
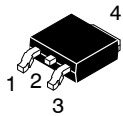


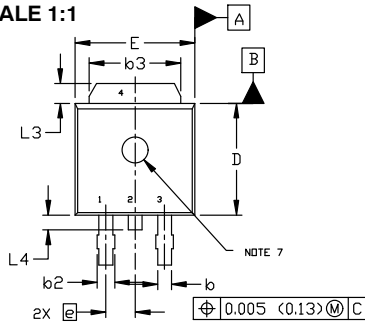
Figure 13. Thermal Response



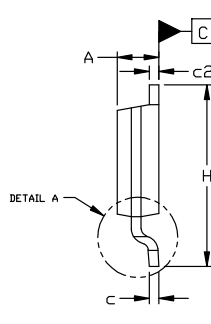
DPAK (SINGLE GAUGE)  
CASE 369C  
ISSUE G

DATE 31 MAY 2023

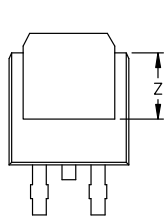
SCALE 1:1



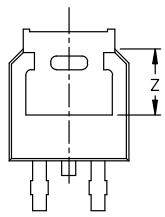
TOP VIEW



SIDE VIEW

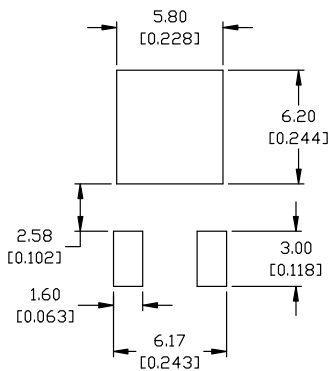


BOTTOM VIEW



BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



RECOMMENDED MOUNTING FOOTPRINT\*

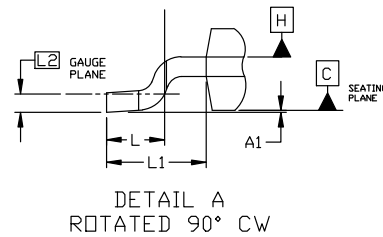
\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

- STYLE 1: PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR
- STYLE 2: PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN
- STYLE 3: PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE
- STYLE 4: PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE
- STYLE 5: PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE
- STYLE 6: PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2
- STYLE 7: PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR
- STYLE 8: PIN 1. N/C  
2. CATHODE  
3. ANODE  
4. CATHODE
- STYLE 9: PIN 1. ANODE  
2. CATHODE  
3. RESISTOR ADJUST  
4. CATHODE
- STYLE 10: PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. ANODE

NOTES:

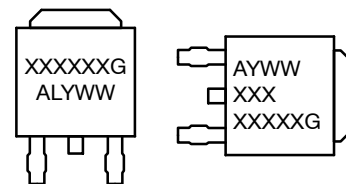
1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---



DETAIL A  
ROTATED 90° CW

GENERIC MARKING DIAGRAM\*



- IC
- Discrete
- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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