

NTGS3A033PZ

MOSFET – Power, Single, P-Channel, TSOP-6 -20 V, -5.9 A

Features

- Leading -20 V Trench for Low $R_{DS(on)}$
- -1.8 V Rated for Low Voltage Gate Drive
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Power Load Switch
- High Side Load Switch
- Charging Circuits and Battery Protection

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DSS}	-20	V	
Gate-to-Source Voltage		V_{GS}	± 8	V	
Continuous Drain Current (Note 1)	Steady State	I_D	$T_A = 25^\circ\text{C}$	-5.1	A
			$T_A = 85^\circ\text{C}$	-3.7	
	$t \leq 5\text{ s}$	$T_A = 25^\circ\text{C}$	-5.9		
Power Dissipation (Note 1)	Steady State	P_D	$T_A = 25^\circ\text{C}$	1.19	W
	$t \leq 5\text{ s}$		1.58		
Continuous Drain Current (Note 2)	Steady State	I_D	$T_A = 25^\circ\text{C}$	-3.8	A
			$T_A = 85^\circ\text{C}$	-2.7	
Power Dissipation (Note 2)		P_D	$T_A = 25^\circ\text{C}$	0.65	W
Pulsed Drain Current	$t_p = 10\ \mu\text{s}$	I_{DM}	-20	A	
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$	
Lead Temperature for Soldering Purposes (1/8 in from case for 10 s)		T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	105	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 5\text{ s}$ (Note 1)	$R_{\theta JA}$	79	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	192	

1. Surface-mounted on FR4 board using 1 in. sq. pad size (Cu area = 1.127 in. sq., 2 oz).
2. Surface-mounted on FR4 board using minimum pad size (Cu area = 0.0775 in. sq.).

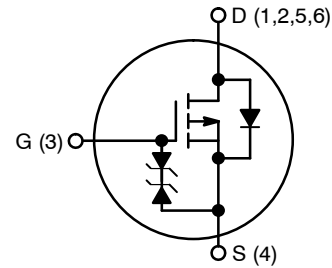


ON Semiconductor®

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$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D MAX
-20 V	22 m Ω @ -4.5 V	-5.9 A
	29 m Ω @ -2.5 V	
	40 m Ω @ -1.8 V	

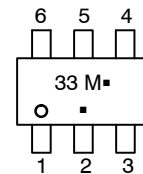
P-Channel MOSFET



MARKING DIAGRAM



TSOP-6
CASE 318G



33 = Specific Device Code
M = Date Code
■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTGS3A033PZT1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTGS3A033PZ

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 μA	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = -250 μA, ref to 25°C		21		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = -20 V	T _J = 25°C		-1	μA
			T _J = 85°C		-10	μA
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V			±10	μA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -250 μA	-0.4		-1.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			3		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -5.1 A		22	33	mΩ
		V _{GS} = -2.5 V, I _D = -4.5 A		29	40	
		V _{GS} = -1.8 V, I _D = -1.5 A		40	55	
Forward Transconductance	g _{FS}	V _{DS} = -5 V, I _D = -5.1 A		23		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = -10 V		1870		pF
Output Capacitance	C _{oss}			203		
Reverse Transfer Capacitance	C _{rss}			174		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -5.1 A		18.8		nC
Threshold Gate Charge	Q _{G(TH)}			1.0		
Gate-to-Source Charge	Q _{GS}			2.7		
Gate-to-Drain Charge	Q _{GD}			5.0		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(on)}	V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -1.0 A, R _G = 6.0 Ω		9.4		ns
Rise Time	t _r			9.3		
Turn-Off Delay Time	t _{d(off)}			131		
Fall Time	t _f			56		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = -1.7 A	T _J = 25°C	-0.7	-1.2	V
			T _J = 125°C	-0.6		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _{SD} /dt = 100 A/μs, I _S = -1.7 A		26		ns
Charge Time	t _a			9.0		
Discharge Time	t _b			17		
Reverse Recovery Charge	Q _{RR}			11		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 ms, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

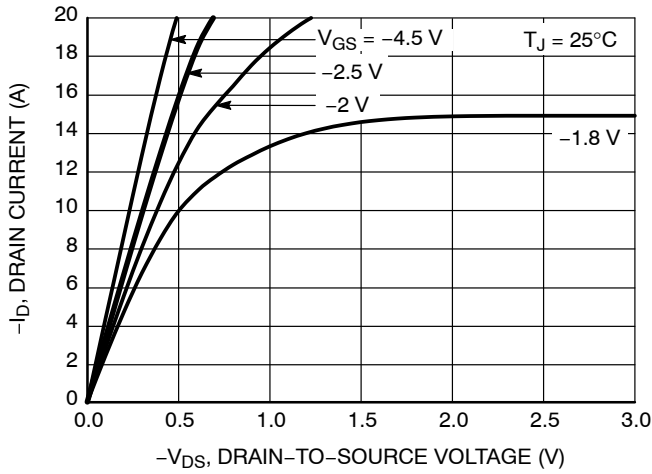


Figure 1. On-Region Characteristics

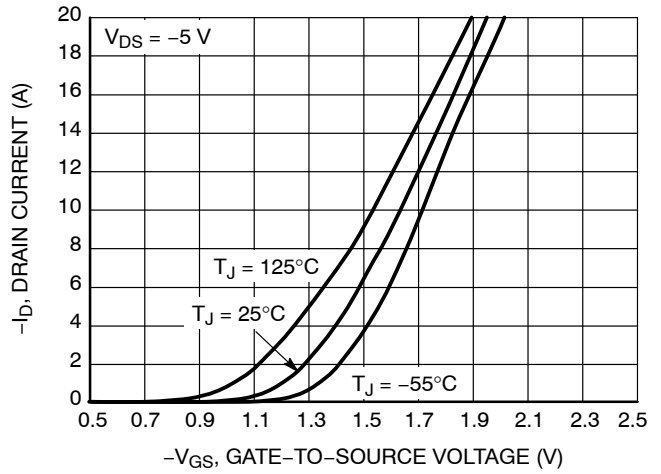


Figure 2. Transfer Characteristics

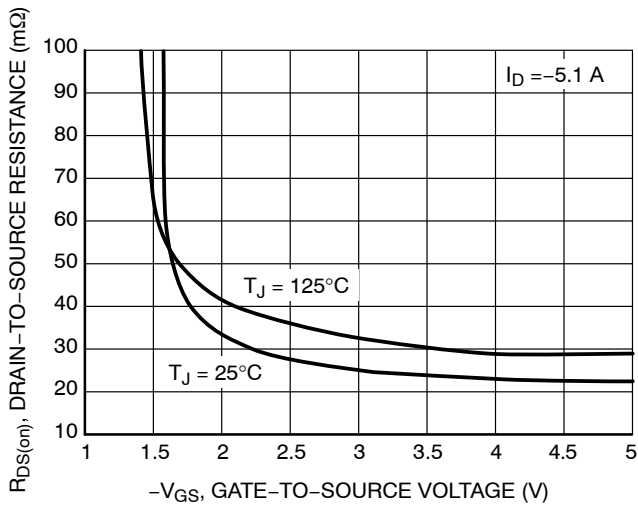


Figure 3. On-Resistance vs. Gate-to-Source Voltage

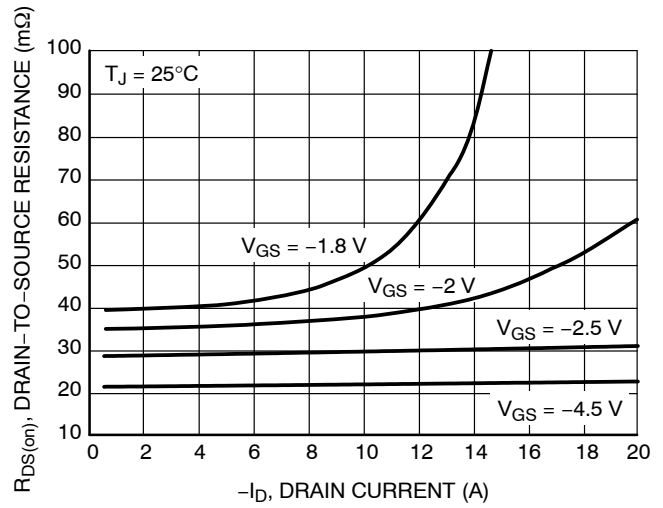


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

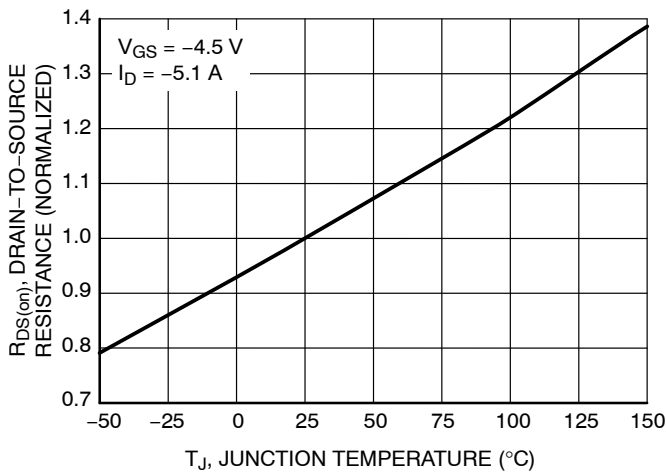


Figure 5. On-Resistance Variation with Temperature

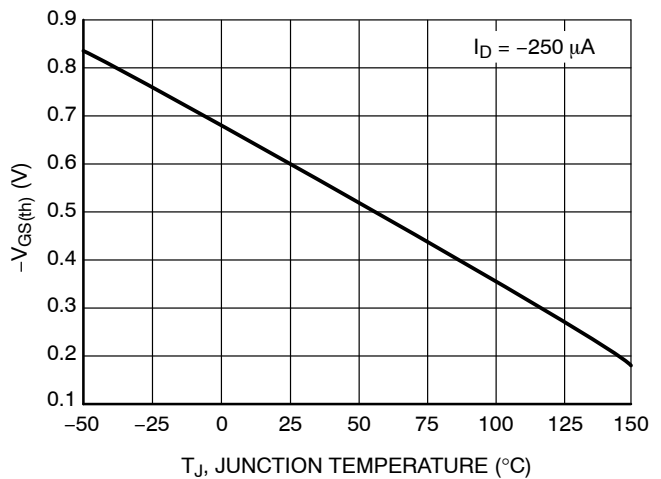


Figure 6. Threshold Voltage Variation with Temperature

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TYPICAL CHARACTERISTICS

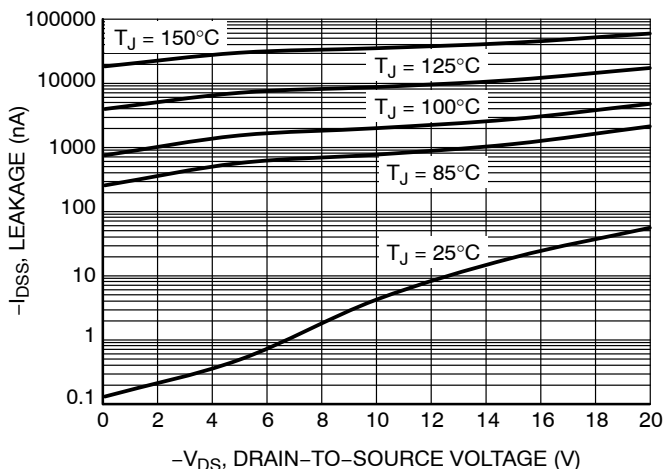


Figure 7. Drain-to-Source Leakage Current vs. Voltage

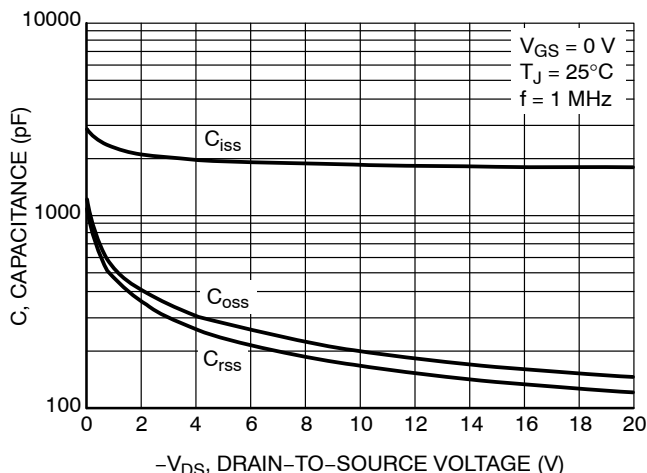


Figure 8. Capacitance Variation

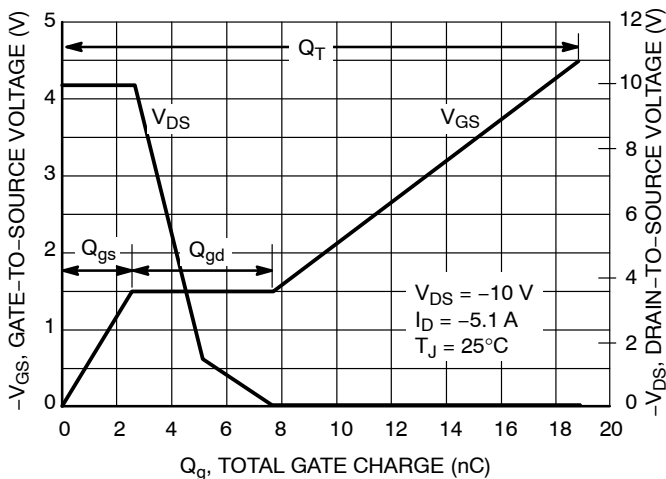


Figure 9. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

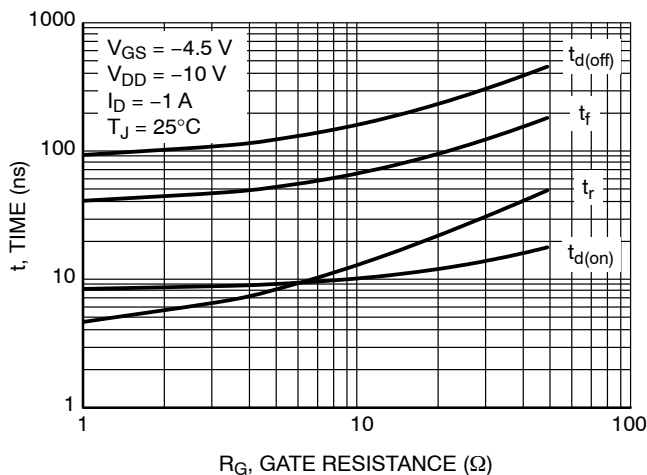


Figure 10. Resistive Switching Time Variation vs. Gate Resistance

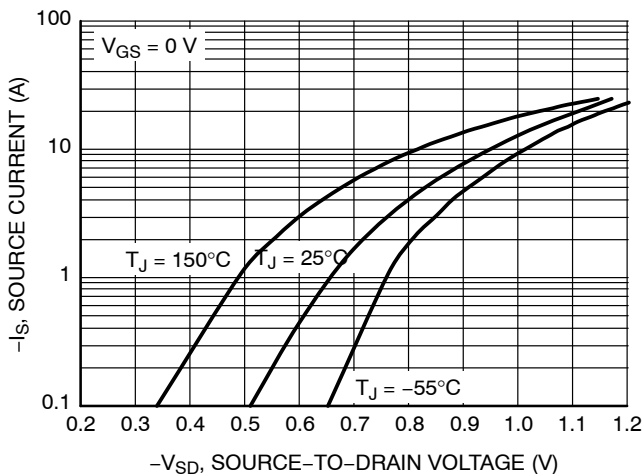


Figure 11. Diode Forward Voltage vs. Current

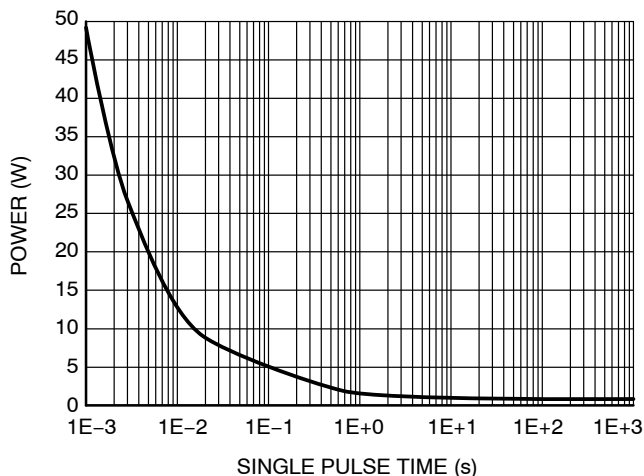


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS

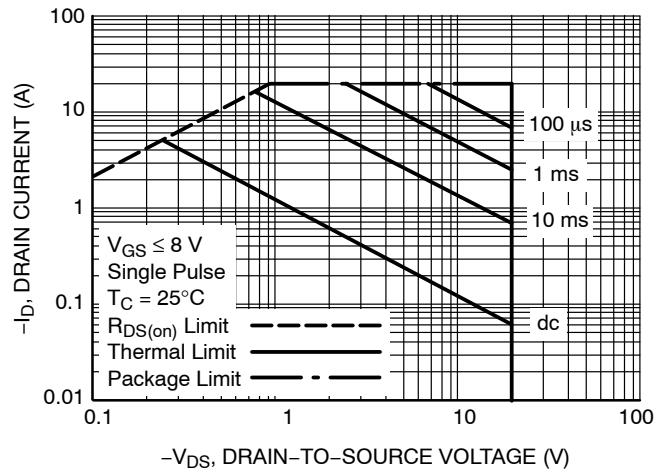


Figure 13. Maximum Rated Forward Biased Safe Operating Area

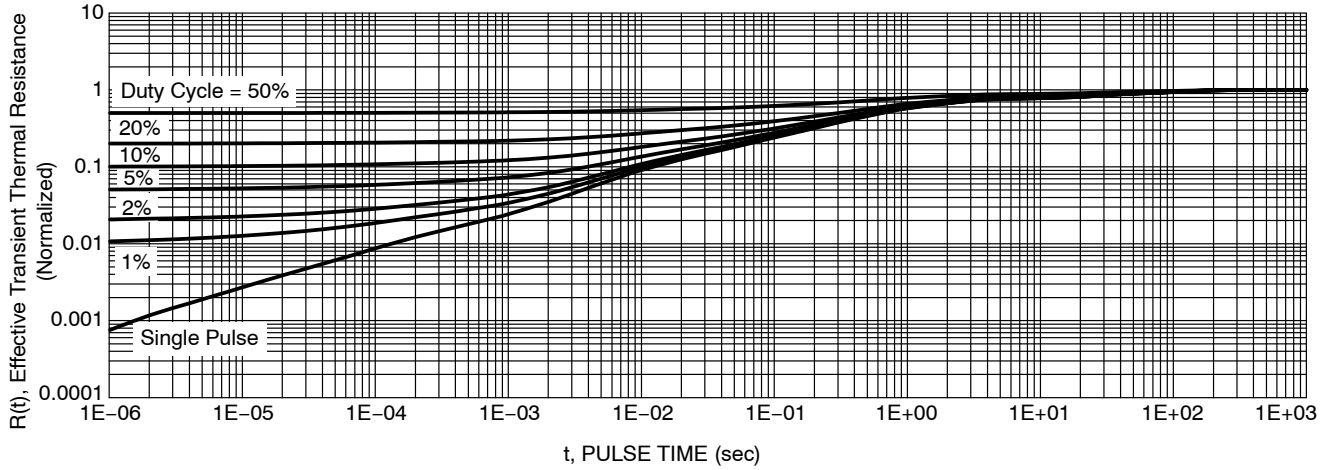


Figure 14. Thermal Response

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



TSOP-6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

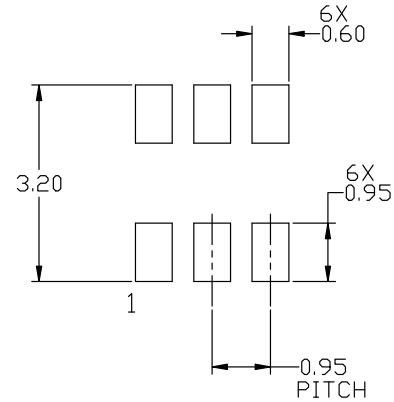
DATE 26 FEB 2024



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



TSOP-6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

- | | | | | | |
|--|--|---|---|---|--|
| <p>STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN</p> | <p>STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2</p> | <p>STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out</p> | <p>STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD</p> | <p>STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2</p> | <p>STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR</p> |
| <p>STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER</p> | <p>STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND</p> | <p>STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE</p> | <p>STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)-
4. D(IN)-
5. VBUS
6. D(IN)+</p> | <p>STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2</p> | <p>STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O</p> |
| <p>STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1</p> | <p>STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN</p> | <p>STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE</p> | <p>STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE</p> | <p>STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR</p> | |

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