

NTHD4P02F

MOSFET – Power, Single, P-Channel, Schottky Diode, ChipFET, Schottky Barrier -20 V, -3.0 A, 3.0 A



ON Semiconductor®

<http://onsemi.com>

Features

- Leadless SMD Package Featuring a MOSFET and Schottky Diode
- 40% Smaller than TSOP-6 Package with Similar Thermal Characteristics
- Independent Pinout to each Device to Ease Circuit Design
- Ultra Low V_F Schottky
- Pb-Free Package is Available

Applications

- Li-Ion Battery Charging
- High Side DC-DC Conversion Circuits
- High Side Drive for Small Brushless DC Motors
- Power Management in Portable, Battery Powered Products

MOSFET MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Units	
Drain-to-Source Voltage	V_{DSS}	-20	V	
Gate-to-Source Voltage	V_{GS}	± 12	V	
Continuous Drain Current	Steady State	$T_J = 25^\circ\text{C}$	-2.2	A
		$T_J = 85^\circ\text{C}$	-1.6	A
	$t \leq 5$ s	$T_J = 25^\circ\text{C}$	-3.0	A
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	-9.0	A
Power Dissipation	Steady State	$T_J = 25^\circ\text{C}$	1.1	W
		$T_J = 85^\circ\text{C}$	0.6	W
	$t \leq 5$ s	$T_J = 25^\circ\text{C}$	2.1	W
Continuous Source Current (Body Diode)	I_S	-2.1	A	
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

SCHOTTKY DIODE MAXIMUM RATINGS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

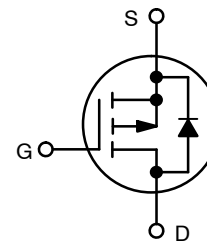
Parameter	Symbol	Value	Units
Peak Repetitive Reverse Voltage	V_{RRM}	20	V
DC Blocking Voltage	V_R	20	V

MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
-20 V	-130 m Ω @ -4.5 V	-3.0 A
	200 m Ω @ -2.5 V	

SCHOTTKY DIODE

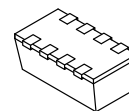
V_R MAX	V_F TYP	I_F MAX
20 V	0.510 V	3.0 A



P-Channel MOSFET

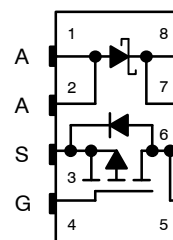


SCHOTTKY DIODE

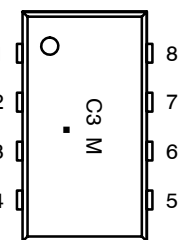


ChipFET
CASE 1206A
STYLE 3

PIN CONNECTIONS



MARKING DIAGRAM



C3 = Specific Device Code
M = Month Code
■ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTHD4P02FT1	ChipFET	3000/Tape & Reel
NTHD4P02FT1G	ChipFET (Pb-free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTHD4P02F

SCHOTTKY DIODE MAXIMUM RATINGS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Units
Average Rectified Forward Current	Steady State	I_F	2.2	A
	$t \leq 5$ s		3.0	A

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Max	Units
Junction-to-Ambient (Note 1)	Steady State	$R_{\theta JA}$	110	$^\circ\text{C/W}$
	$t \leq 5$ s		60	

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
-----------	--------	-----------------	-----	-----	-----	-------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = -250$ μA	-20	-23		V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16$ V, $V_{GS} = 0$ V, $T_J = 25^\circ\text{C}$			-1.0	μA
		$V_{DS} = -16$ V, $V_{GS} = 0$ V, $T_J = 85^\circ\text{C}$			-5.0	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 12$ V			± 100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = -250$ μA	-0.6	-0.75	-1.2	V
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5$ V, $I_D = -2.2$ A		0.130	0.155	Ω
		$V_{GS} = -2.5$ V, $I_D = -1.7$ A		0.200	0.240	
Forward Transconductance	g_{FS}	$V_{DS} = -10$ V, $I_D = -1.7$ A		5.0		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0$ V, $f = 1.0$ MHz, $V_{DS} = -10$ V		185	300	pF
Output Capacitance	C_{OSS}			95	150	
Reverse Transfer Capacitance	C_{RSS}			30	50	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5$ V, $V_{DS} = -10$ V, $I_D = -2.2$ A		3.0	6.0	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.2		
Gate-to-Source Charge	Q_{GS}			0.5		
Gate-to-Drain Charge	Q_{GD}			0.9		

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5$ V, $V_{DD} = -16$ V, $I_D = -2.2$ A, $R_G = 2.5$ Ω		7.0	12	ns
Rise Time	t_r			13	25	
Turn-Off Delay Time	$t_{d(OFF)}$			33	50	
Fall Time	t_f			27	40	

DRAIN-SOURCE DIODE CHARACTERISTICS (Note 2)

Forward Diode Voltage	V_{SD}	$V_{GS} = 0$ V, $I_S = -2.1$ A		-0.85	-1.15	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0$ V, $I_S = -2.1$ A, $dI_S/dt = 100$ A/ μs		32		ns
Charge Time	t_a			10		
Discharge Time	t_b			22		
Reverse Recovery Charge	Q_{RR}			15		

SCHOTTKY DIODE ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
-----------	--------	-----------------	-----	-----	-----	-------

NTHD4P02F

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
-----------	--------	-----------------	-----	-----	-----	-------

SCHOTTKY DIODE ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Maximum Instantaneous Forward Voltage	V_F	$I_F = 0.1 \text{ A}$		0.425		V
		$I_F = 0.5 \text{ A}$		0.480		
		$I_F = 1.0 \text{ A}$		0.510	0.575	
Maximum Instantaneous Reverse Current	I_R	$V_R = 10 \text{ V}$			1.0	μA
		$V_R = 20 \text{ V}$			5.0	
Maximum Voltage Rate of Change	dv/dt	$V_R = 20 \text{ V}$		10,000		V/ns
Non-Repetitive Peak Surge Current	I_{FSM}	Halfwave, Single Pulse, 60 Hz			23	A

2. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.
3. Switching characteristics are independent of operating junction temperatures.

NTHD4P02F

TYPICAL MOSFET PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

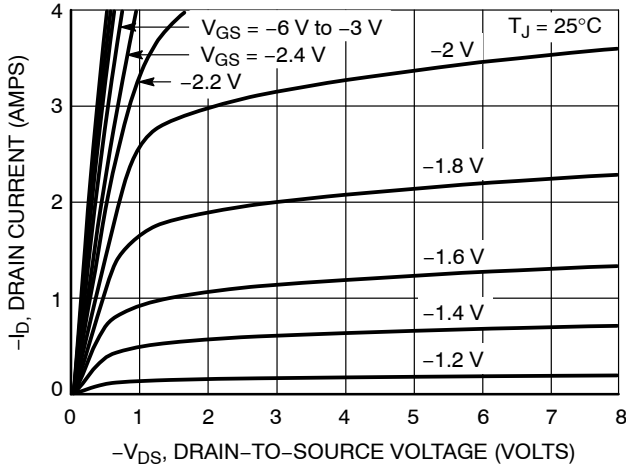


Figure 1. On-Region Characteristics

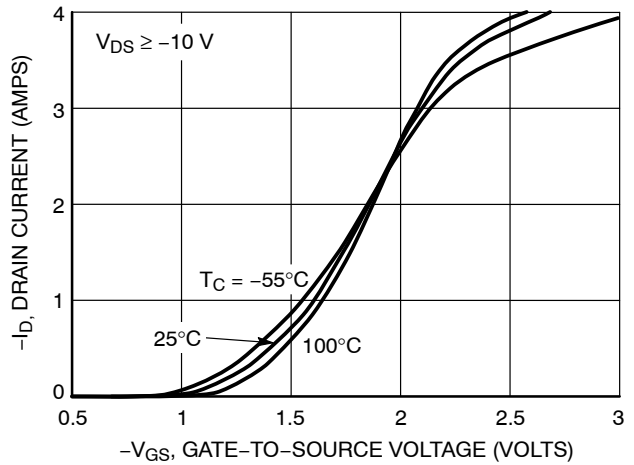


Figure 2. Transfer Characteristics

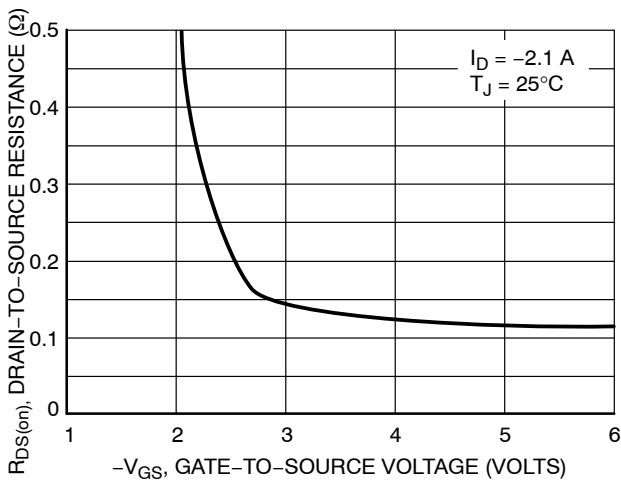


Figure 3. On-Resistance vs. Gate-to-Source Voltage

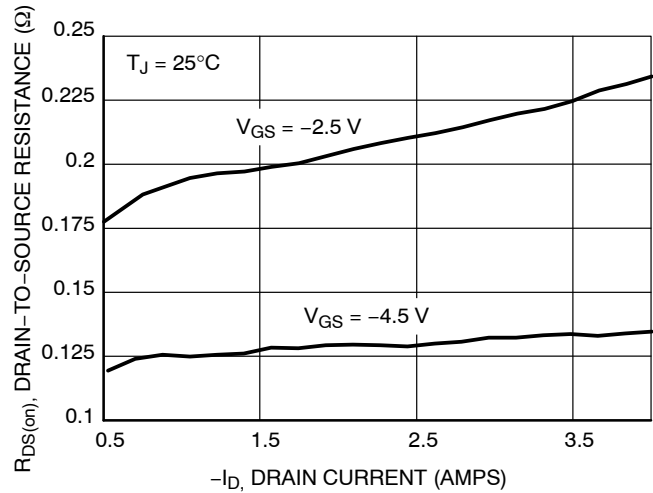


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

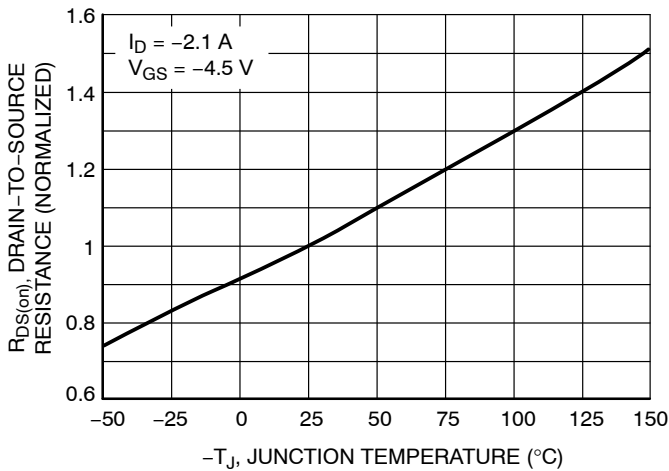


Figure 5. On-Resistance Variation with Temperature

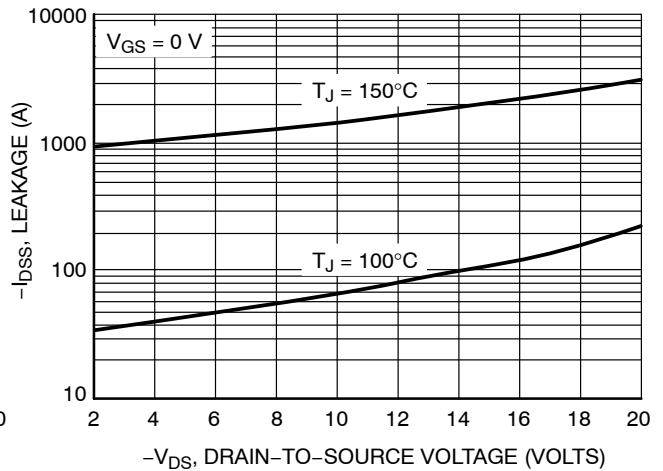
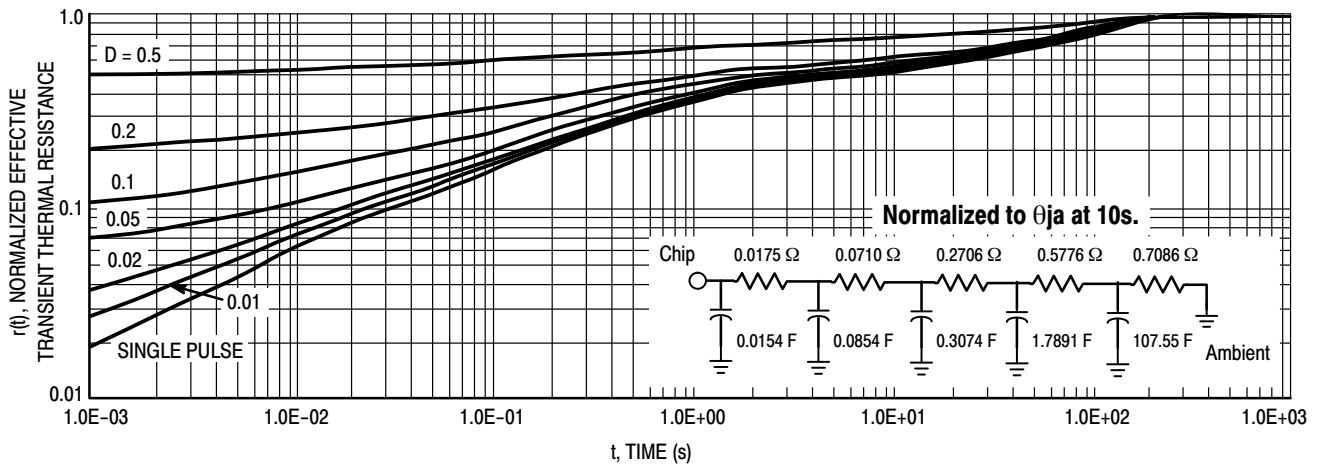
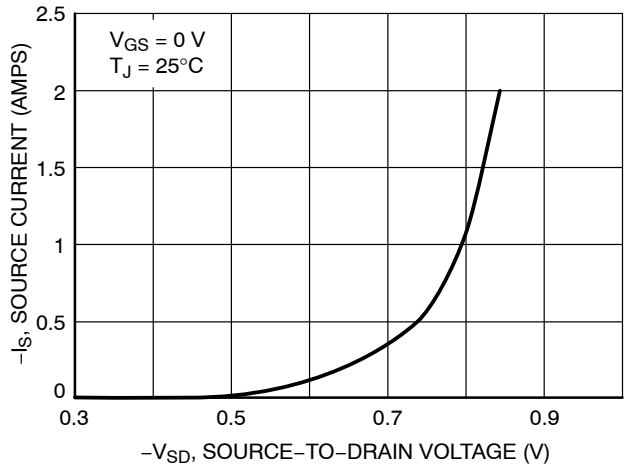
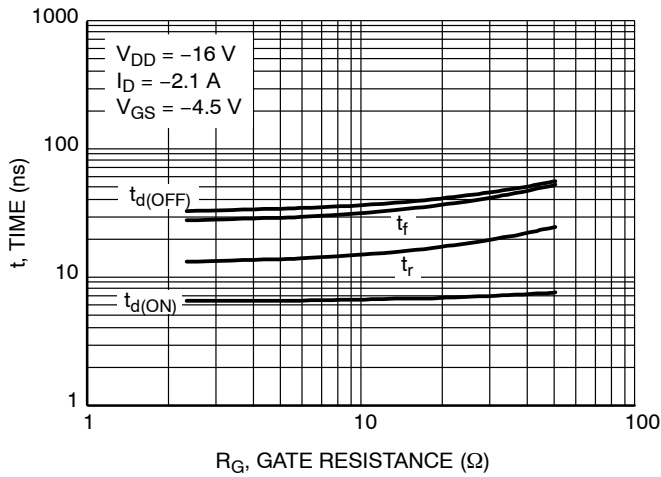
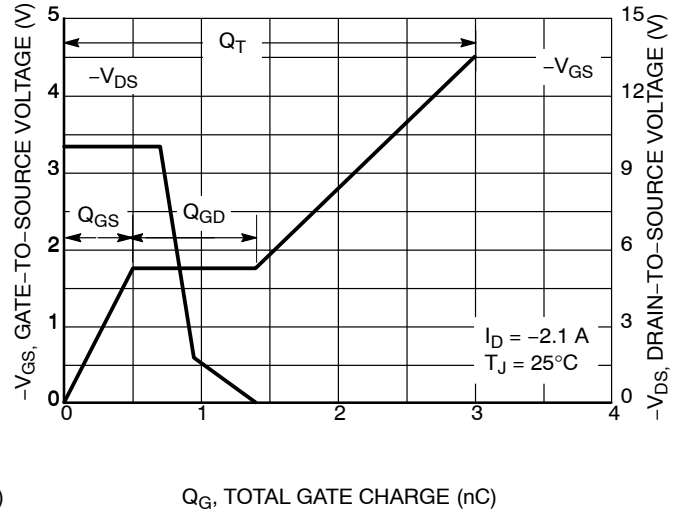
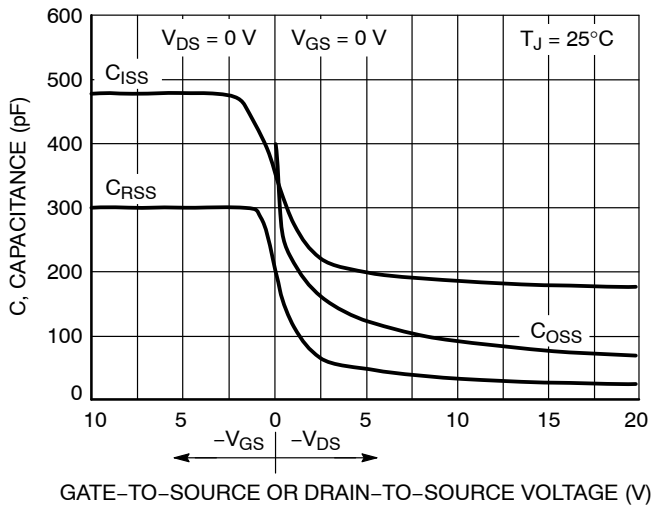


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NTHD4P02F

TYPICAL MOSFET PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)



NTHD4P02F

TYPICAL SCHOTTKY PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

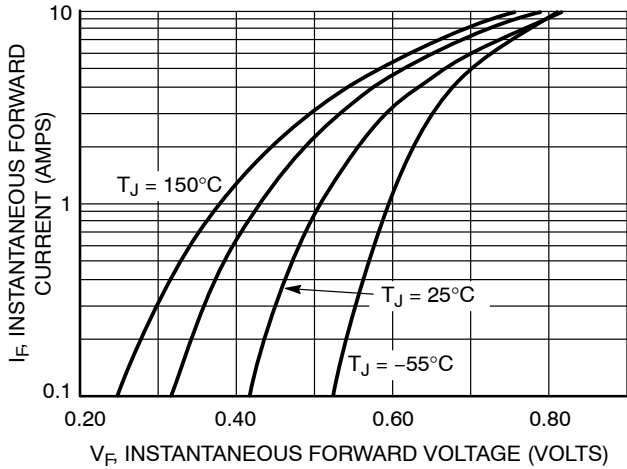


Figure 12. Typical Forward Voltage

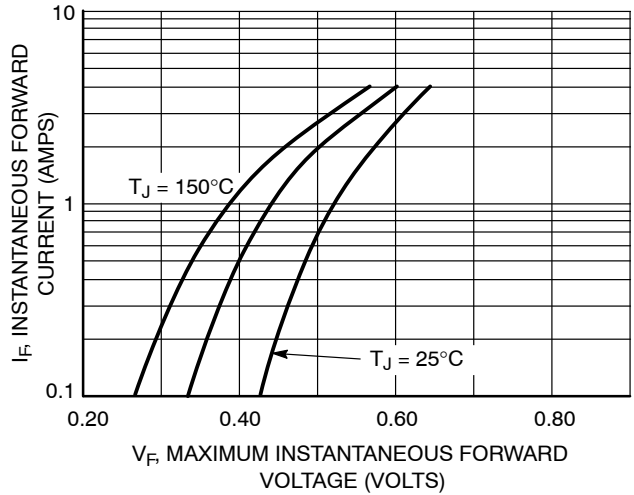


Figure 13. Maximum Forward Voltage

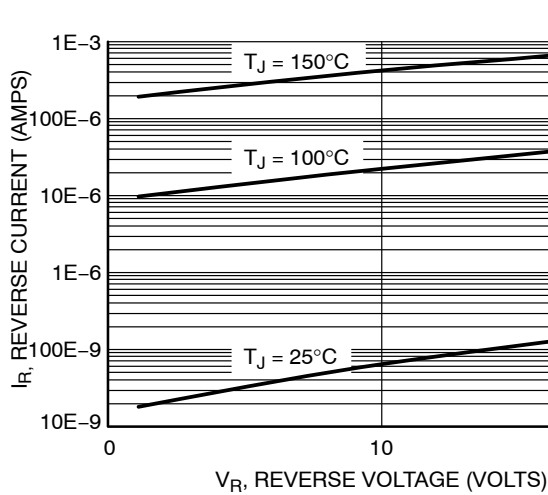


Figure 14. Typical Reverse Current

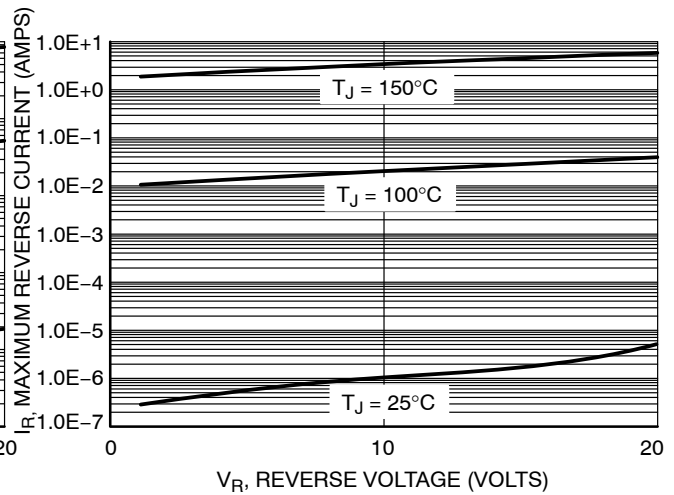


Figure 15. Maximum Reverse Current

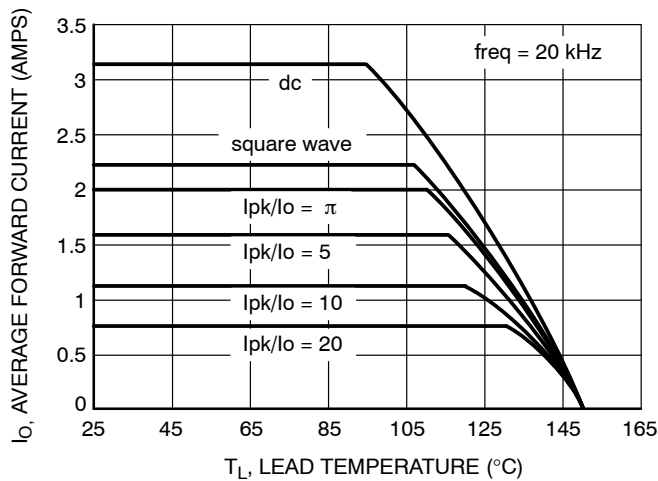


Figure 16. Current Derating

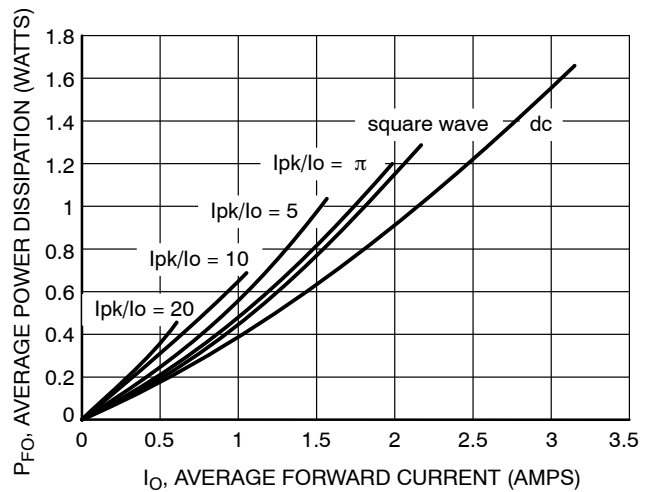


Figure 17. Forward Power Dissipation

NTHD4P02F

SOLDERING FOOTPRINT*

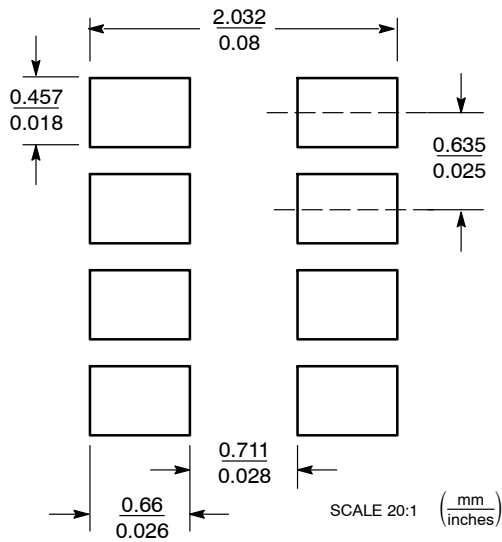


Figure 18. Basic

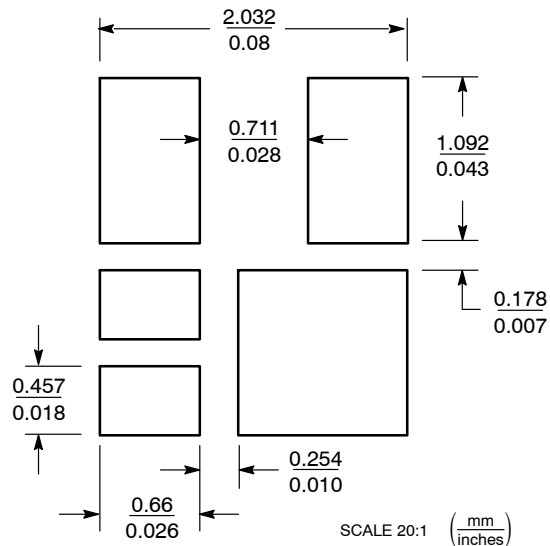


Figure 19. Style 3

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 18. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 19 improves the thermal area of the drain connections (pins 5, 6) while remaining within the confines

of the basic footprint. The drain copper area is 0.0019 sq. in. (or 1.22 sq. mm). This will assist the power dissipation path away from the device (through the copper lead-frame) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

MECHANICAL CASE OUTLINE

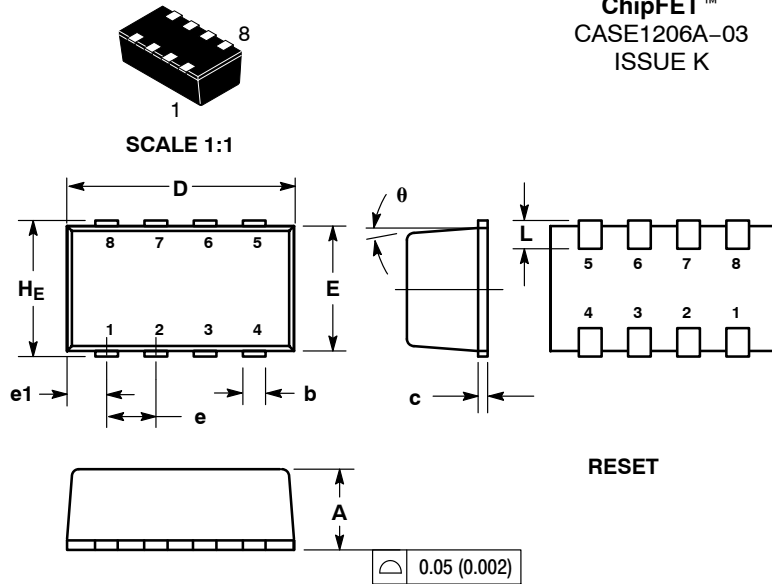
PACKAGE DIMENSIONS

ON Semiconductor®



ChipFET™
CASE1206A-03
ISSUE K

DATE 19 MAY 2009

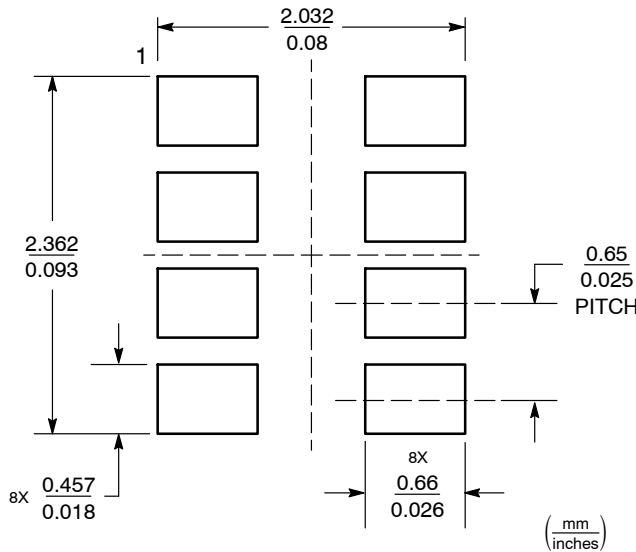


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

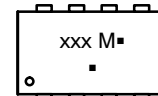
- | | | | | | |
|--|--|--|---|--|--|
| STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN | STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1 | STYLE 3:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE | STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR | STYLE 5:
PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE | STYLE 6:
PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN |
|--|--|--|---|--|--|

SOLDERING FOOTPRINT



Basic Style

GENERIC MARKING DIAGRAM*



- xxx = Specific Device Code
 - M = Month Code
 - = Pb-Free Package
- (Note: Microdot may be in either location)

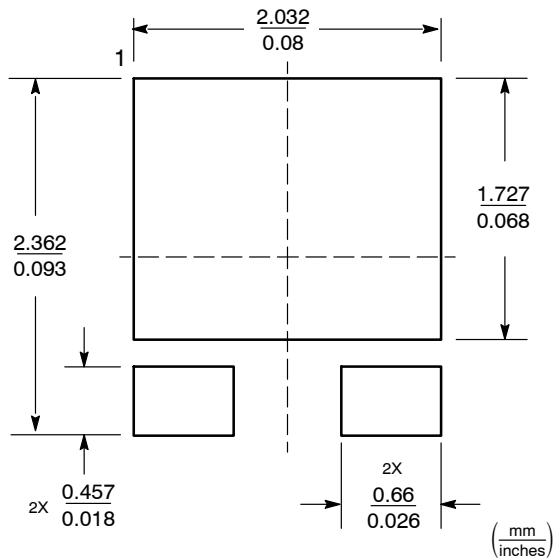
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

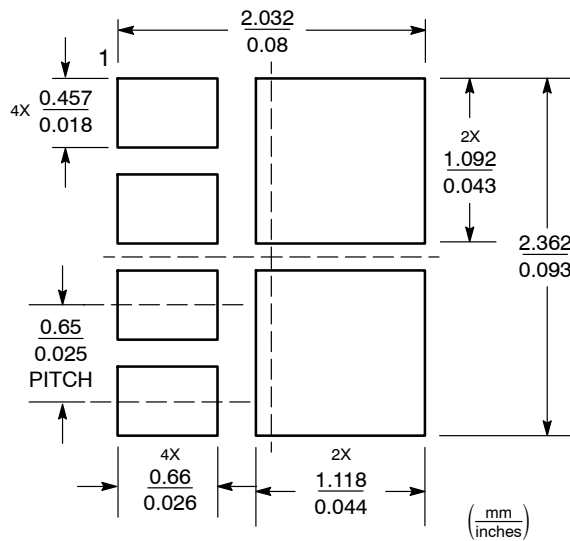
DOCUMENT NUMBER:	98AON03078D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	ChipFET	PAGE 1 OF 2

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

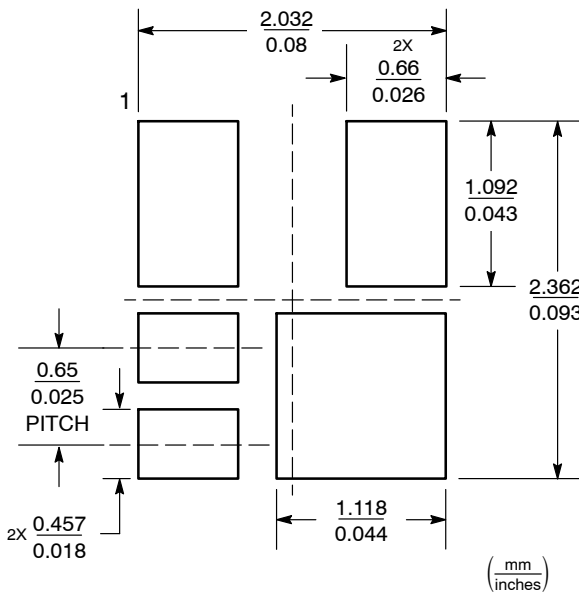
ADDITIONAL SOLDERING FOOTPRINTS*



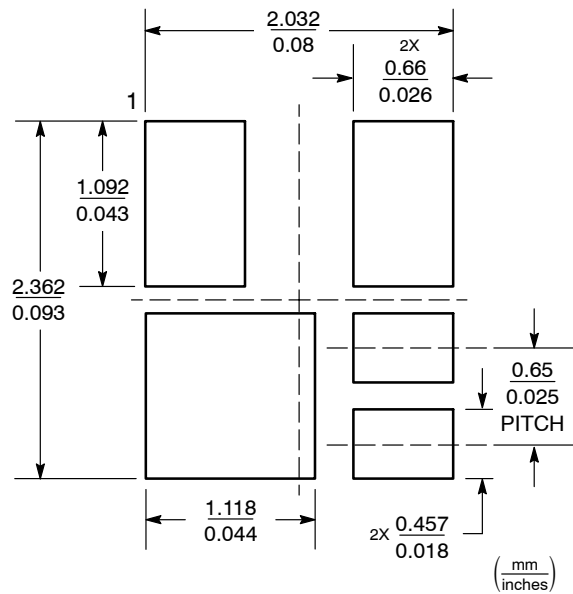
Styles 1 and 4



Style 2



Style 3



Style 5

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON03078D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	ChipFET	PAGE 2 OF 2

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

