

NTLUS030N03C

MOSFET – Power, Single, N-Channel, μ Cool, UDFN6, 1.6x1.6x0.55 mm 30 V, 18 m Ω , 6.9 A



ON Semiconductor®

www.onsemi.com

Features

- UDFN Package with Exposed Drain Pads for Excellent Thermal Conduction
- Low Profile UDFN 1.6 x 1.6 x 0.55 mm for Board Space Saving
- Ultra Low $R_{DS(on)}$
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Power Load Switch
- Wireless Charging
- DC-DC Converters
- Motor Drive

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	30	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D 6.9	A
		$T_A = 85^\circ\text{C}$	5.0	
		$T_A = 25^\circ\text{C}$	P_D 1.49	W
Continuous Drain Current $R_{\theta JA}$ (Note 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D 4.5	A
		$T_A = 85^\circ\text{C}$	3.2	
		$T_A = 25^\circ\text{C}$	P_D 0.64	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM} 20	A	
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

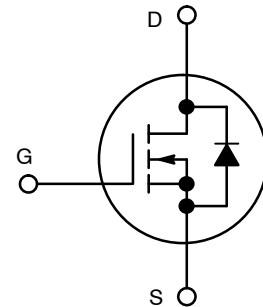
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1, 3)	$R_{\theta JA}$	83.7	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State min Pad (Note 2, 3)	$R_{\theta JA}$	196.6	

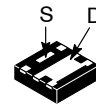
1. Surface-mounted on FR4 board using 1 in² pad size, 2 oz Cu pad.

MOSFET		
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
30 V	18 m Ω @ 10 V	6.9 A
	26 m Ω @ 4.5 V	

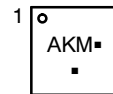


N-CHANNEL MOSFET

MARKING DIAGRAM



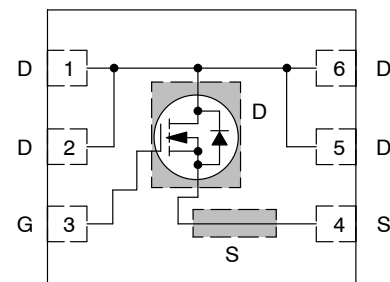
UDFN6
(μ COOL)
CASE 517AU



AK = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

NTLUS030N03C

- Surface-mounted on FR4 board using the min pad size, 2 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- This device does not have ESD protection diode.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}, \text{ref to } 25^\circ\text{C}$		14.2		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.2		2.2	V
Negative Threshold Temp. Coefficient	$V_{GS(TH)}/T_J$	$I_D = 250\ \mu\text{A}, \text{ref to } 25^\circ\text{C}$		-4.1		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 6.0\text{ A}$		14	18	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 5.0\text{ A}$		20	26	
Forward Transconductance	g_{FS}	$V_{DS} = 1.5\text{ V}, I_D = 5.0\text{ A}$		16		S

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 15\text{ V}$		400		pF
Output Capacitance	C_{OSS}			215		
Reverse Transfer Capacitance	C_{RSS}			21		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 5.0\text{ A}$		3.7		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.6		
Gate-to-Source Charge	Q_{GS}			1.3		
Gate-to-Drain Charge	Q_{GD}			1.2		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}; I_D = 5.0\text{ A}$		8		nC

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 15\text{ V}, I_D = 5.0\text{ A}, R_G = 6\ \Omega$		9		ns
Rise Time	t_r			15		
Turn-Off Delay Time	$t_{d(OFF)}$			11		
Fall Time	t_f			2.5		

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DD} = 15\text{ V}, I_D = 5.0\text{ A}, R_G = 6\ \Omega$		6		ns
Rise Time	t_r			13		
Turn-Off Delay Time	$t_{d(OFF)}$			14		
Fall Time	t_f			2		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 5.0\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.0	V
			$T_J = 125^\circ\text{C}$		0.7		

- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

NTLUS030N03C

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}$, $di/dt = 100\text{ A}/\mu\text{s}$, $I_S = 5.0\text{ A}$		20		ns
Charge Time	t_a			11		
Discharge Time	t_b			10		
Reverse Recovery Charge	Q_{RR}			8		nC

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

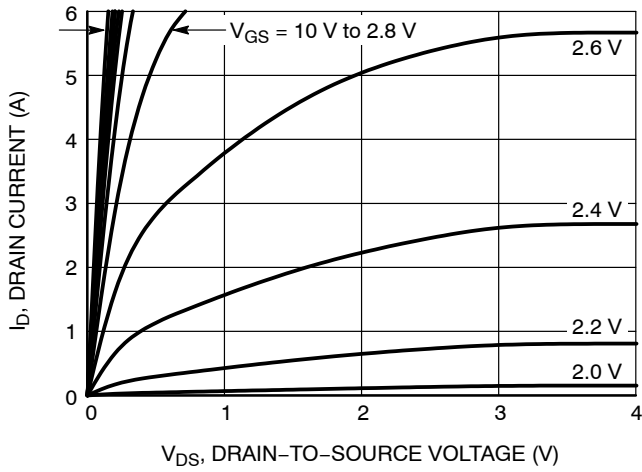


Figure 1. On-Region Characteristics

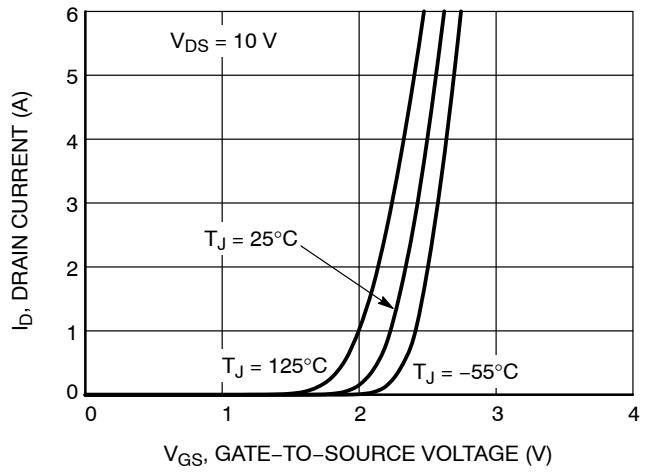


Figure 2. Transfer Characteristics

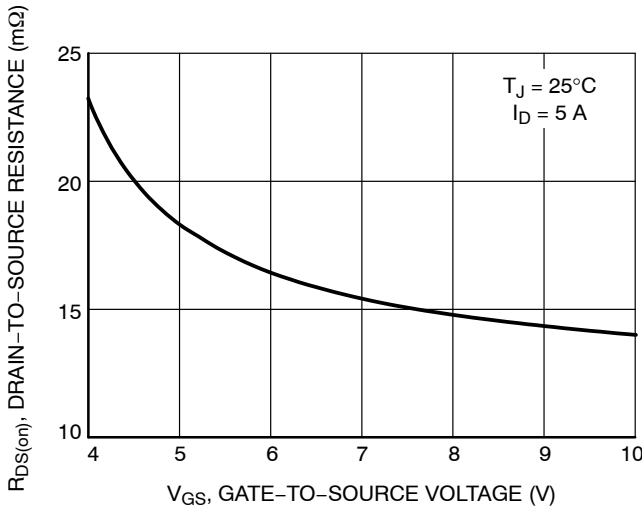


Figure 3. On-Resistance vs. Gate-to-Source Voltage

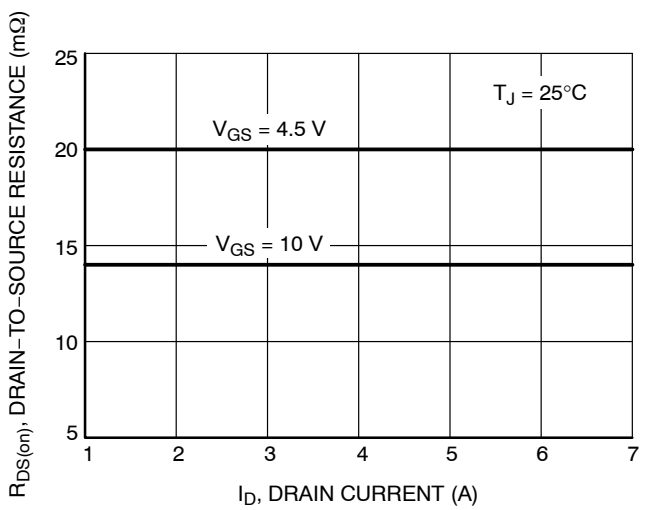


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

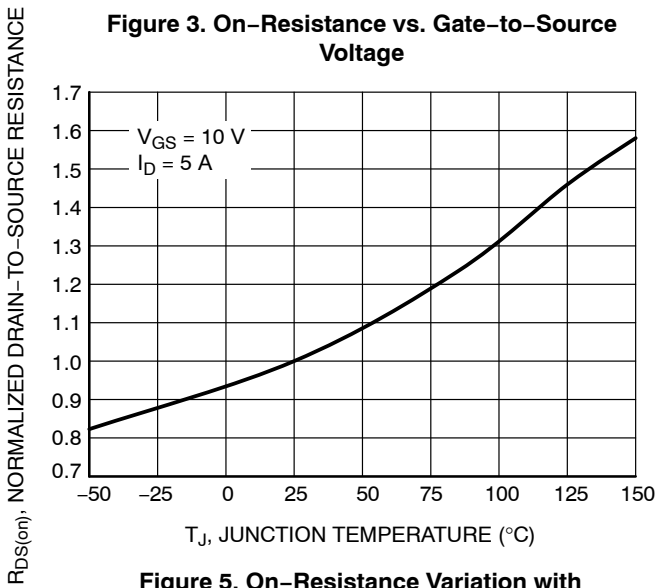


Figure 5. On-Resistance Variation with Temperature

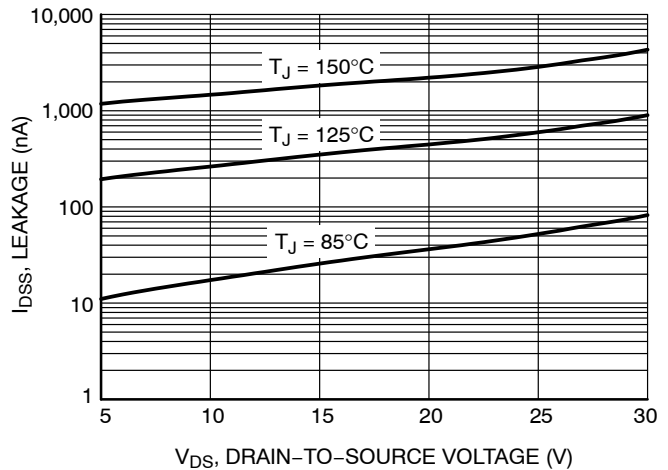


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

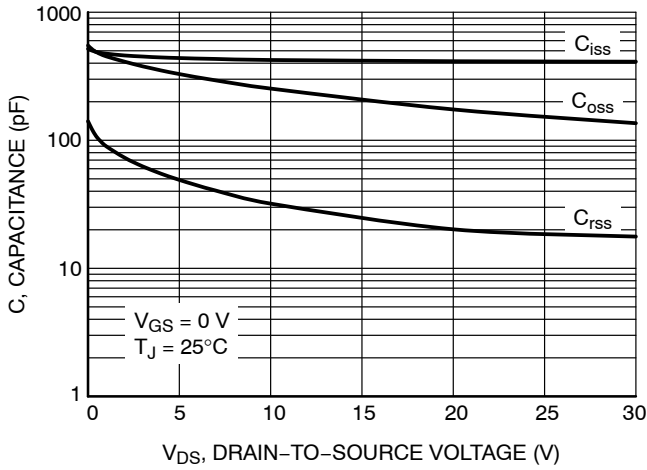


Figure 7. Capacitance Variation

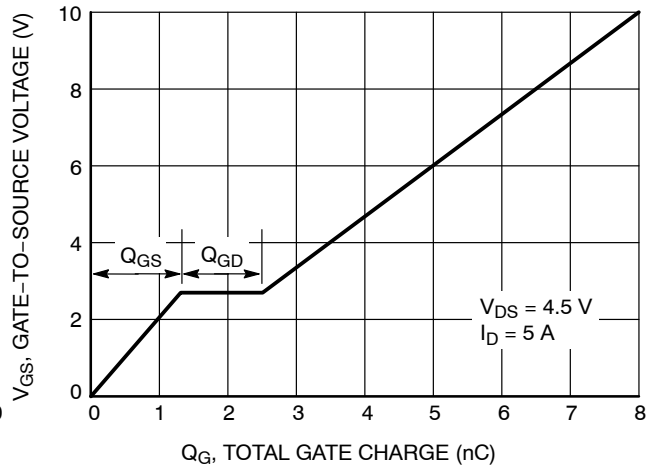


Figure 8. Gate-to-Source vs. Total Charge

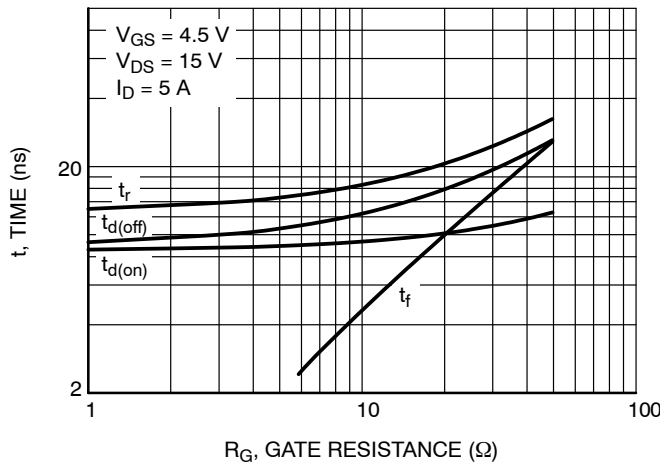


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

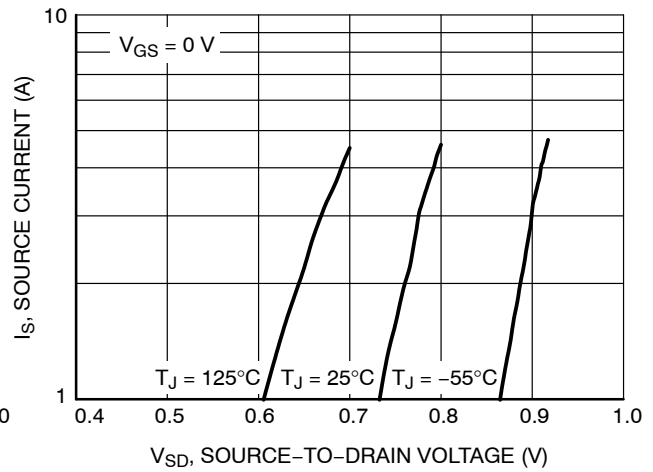


Figure 10. Diode Forward Voltage vs. Current

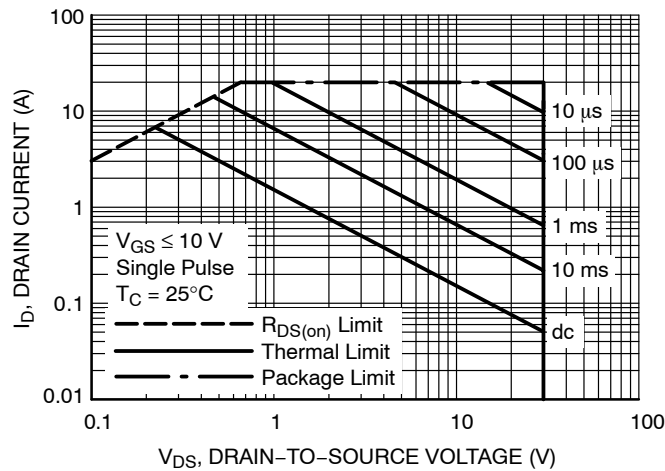


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL CHARACTERISTICS

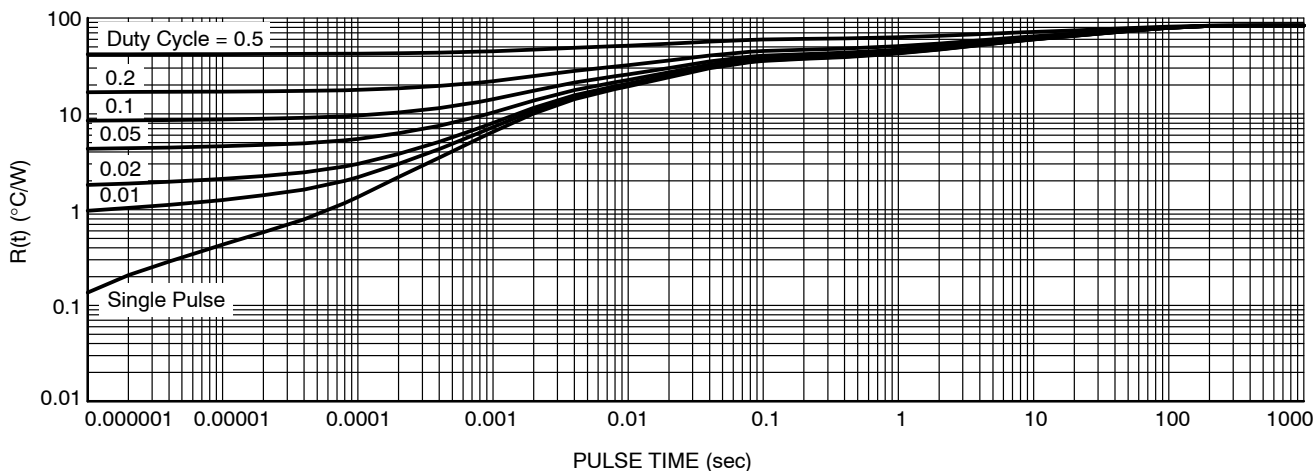


Figure 12. Thermal Response

DEVICE ORDERING INFORMATION

Device	Package	Shipping [†]
NTLUS030N03CTAG	UDFN6 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

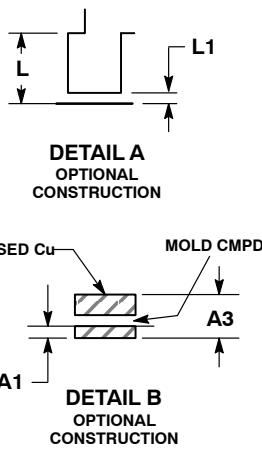
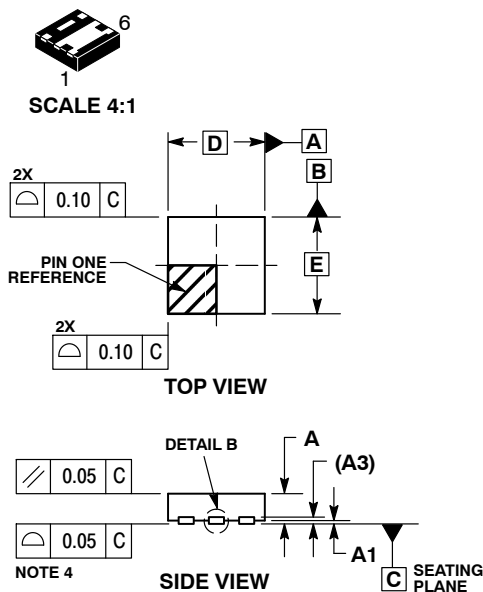
PACKAGE DIMENSIONS

ON Semiconductor®



UDFN6 1.6x1.6, 0.5P CASE 517AU-01 ISSUE O

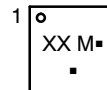
DATE 16 OCT 2008



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.20	0.30
D	1.60	BSC
E	1.60	BSC
e	0.50	BSC
D1	0.62	0.72
D2	0.15	0.25
E2	0.57	0.67
F	0.55	BSC
G	0.25	BSC
L	0.20	0.30
L1	---	0.15

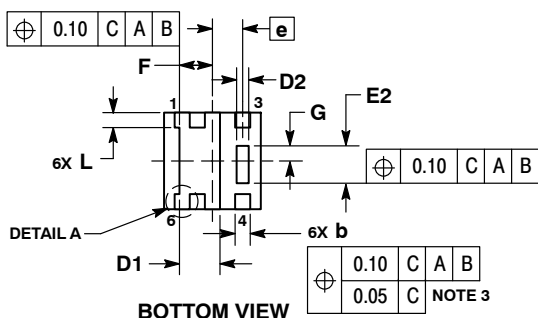
GENERIC MARKING DIAGRAM*



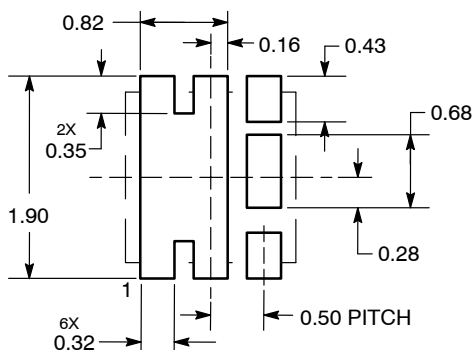
XX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.



SOLDERMASK DEFINED MOUNTING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	UDFN6, 1.6X1.6, 0.5P	PAGE 1 OF 1

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