

NTMFS4983NF

Power MOSFET

30 V, 106 A, Single N-Channel, SO-8 FL

Features

- Integrated Schottky Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- CPU Power Delivery
- Synchronous Rectification for DC-DC Converters
- Low Side Switching
- Telecom Secondary Side Rectification

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

| Parameter | Symbol | Value | Unit | | |
|--|--------------------------|--------------------------|------------------|-----|---|
| Drain-to-Source Voltage | V_{DSS} | 30 | V | | |
| Gate-to-Source Voltage | V_{GS} | ± 20 | V | | |
| Continuous Drain Current $R_{\theta JA}$ (Note 1) | I_D | $T_A = 25^\circ\text{C}$ | 30 | | |
| | | $T_A = 85^\circ\text{C}$ | 22 | | |
| Power Dissipation $R_{\theta JA}$ (Note 1) | P_D | $T_A = 25^\circ\text{C}$ | 3.13 | | |
| | | $T_A = 85^\circ\text{C}$ | | | |
| Continuous Drain Current $R_{\theta JA} \leq 10$ sec | I_D | $T_A = 25^\circ\text{C}$ | 48 | | |
| | | $T_A = 85^\circ\text{C}$ | 34 | | |
| Power Dissipation $R_{\theta JA}, t \leq 10$ sec | P_D | $T_A = 25^\circ\text{C}$ | 7.7 | | |
| | | $T_A = 85^\circ\text{C}$ | | | |
| Continuous Drain Current $R_{\theta JA}$ (Note 2) | I_D | $T_A = 25^\circ\text{C}$ | 22 | | |
| | | $T_A = 85^\circ\text{C}$ | 16 | | |
| Power Dissipation $R_{\theta JA}$ (Note 2) | P_D | $T_A = 25^\circ\text{C}$ | 1.7 | | |
| | | $T_A = 85^\circ\text{C}$ | | | |
| Continuous Drain Current $R_{\theta JC}$ (Note 1) | I_D | $T_C = 25^\circ\text{C}$ | 106 | | |
| | | $T_C = 85^\circ\text{C}$ | 76 | | |
| Power Dissipation $R_{\theta JC}$ (Note 1) | P_D | $T_C = 25^\circ\text{C}$ | 38 | | |
| | | $T_C = 85^\circ\text{C}$ | | | |
| Pulsed Drain Current | $t_p = 10\mu\text{s}$ | $T_A = 25^\circ\text{C}$ | I_{DM} | 320 | A |
| Current limited by package | $T_A = 25^\circ\text{C}$ | $I_{Dmaxpkg}$ | 100 | A | |
| Operating Junction and Storage Temperature | T_J, T_{STG} | -55 to +150 | $^\circ\text{C}$ | | |
| Source Current (Body Diode) | I_S | 54 | A | | |
| Drain to Source dV/dt | dV/dt | 6 | V/ns | | |
| Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 50$ V, $V_{GS} = 10$ V, $I_L = 45$ A _{pk} , $L = 0.1$ mH, $R_G = 25$ Ω) | EAS | 101 | mJ | | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | T_L | 260 | $^\circ\text{C}$ | | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

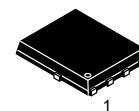
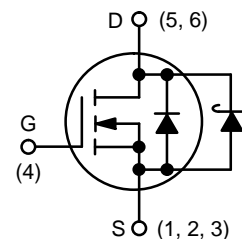


ON Semiconductor®

www.onsemi.com

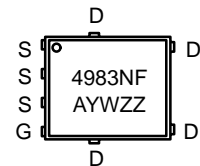
| $V_{(BR)DSS}$ | $R_{DS(ON)}$ MAX | I_D MAX |
|---------------|------------------------|-----------|
| 30 V | 2.1 m Ω @ 10 V | 106 A |
| | 3.1 m Ω @ 4.5 V | |

N-CHANNEL MOSFET



SO-8 FLAT LEAD
CASE 488AA
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|------------------|--------------------|
| NTMFS4983NFT1G | SO-8FL (Pb-Free) | 1500 / Tape & Reel |
| NTMFS4983NFT3G | SO-8FL (Pb-Free) | 5000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTMFS4983NF

THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|------|
| Junction-to-Case (Drain) | $R_{\theta JC}$ | 3.3 | °C/W |
| Junction-to-Ambient – Steady State (Note 1) | $R_{\theta JA}$ | 40 | |
| Junction-to-Ambient – Steady State (Note 2) | $R_{\theta JA}$ | 74 | |
| Junction-to-Ambient – $t \leq 10$ sec | $R_{\theta JA}$ | 16.3 | |

- Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu.
- Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm².

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|---|-------------------|--|----|----|-----------|---------------|
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0\text{ V}, I_D = 1.0\text{ mA}$ | 30 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | $I_D = 10\text{ mA}$, referenced to 25°C | | 15 | | mV/°C |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$ $T_J = 25^\circ\text{C}$ | | | 500 | μA |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$ | | | ± 100 | nA |

ON CHARACTERISTICS (Note 3)

| | | | | | | | |
|--|------------------|---|---------------------|-----|-----|-------|------------|
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}, I_D = 1.0\text{ mA}$ | 1.2 | 1.7 | 2.3 | V | |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | $I_D = 10\text{ mA}$, referenced to 25°C | | 5.0 | | mV/°C | |
| Drain-to-Source On Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 30\text{ A}$ | | 1.6 | 2.1 | m Ω |
| | | | $I_D = 15\text{ A}$ | | 1.6 | | |
| | | $V_{GS} = 4.5\text{ V}$ | $I_D = 30\text{ A}$ | | 2.5 | 3.1 | |
| | | | $I_D = 15\text{ A}$ | | 2.5 | | |
| Forward Transconductance | g_{FS} | $V_{DS} = 1.5\text{ V}, I_D = 15\text{ A}$ | | 60 | | S | |

CHARGES AND CAPACITANCES

| | | | | | | |
|------------------------------|--------------|--|--|------|--|----|
| Input Capacitance | C_{ISS} | $V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 15\text{ V}$ | | 3250 | | pF |
| Output Capacitance | C_{OSS} | | | 1340 | | |
| Reverse Transfer Capacitance | C_{RSS} | | | 90 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$ | | 22.6 | | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | 2.9 | | |
| Gate-to-Source Charge | Q_{GS} | | | 7.0 | | |
| Gate-to-Drain Charge | Q_{GD} | | | 6.9 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$ | | 47.9 | | nC |

SWITCHING CHARACTERISTICS (Note 4)

| | | | | | | |
|---------------------|--------------|---|--|------|--|----|
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$ | | 13.5 | | ns |
| Rise Time | t_r | | | 24.9 | | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | 28.7 | | |
| Fall Time | t_f | | | 10.7 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

NTMFS4983NF

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------|---|-----|------|-----|------|
| SWITCHING CHARACTERISTICS (Note 4) | | | | | | |
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$ | | 9.4 | | ns |
| Rise Time | t_r | | | 16.7 | | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | 35.2 | | |
| Fall Time | t_f | | | 7.4 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-------------------------|----------|--|---------------------------|----|------|-----|---|
| Forward Diode Voltage | V_{SD} | $V_{GS} = 0\text{ V},$ $I_S = 2\text{ A}$ | $T_J = 25^\circ\text{C}$ | | 0.4 | 0.7 | V |
| | | | $T_J = 125^\circ\text{C}$ | | 0.32 | | |
| Reverse Recovery Time | t_{RR} | $V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 2\text{ A}$ | | 45 | | ns | |
| Charge Time | t_a | | | 23 | | | |
| Discharge Time | t_b | | | 22 | | | |
| Reverse Recovery Charge | Q_{RR} | | | 50 | | nC | |

PACKAGE PARASITIC VALUES

| | | | | | | |
|-------------------|-------|--------------------------|--|------|--|----------|
| Source Inductance | L_S | $T_A = 25^\circ\text{C}$ | | 0.65 | | nH |
| Drain Inductance | L_D | | | 0.20 | | |
| Gate Inductance | L_G | | | 1.5 | | |
| Gate Resistance | R_G | | | 1.0 | | Ω |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

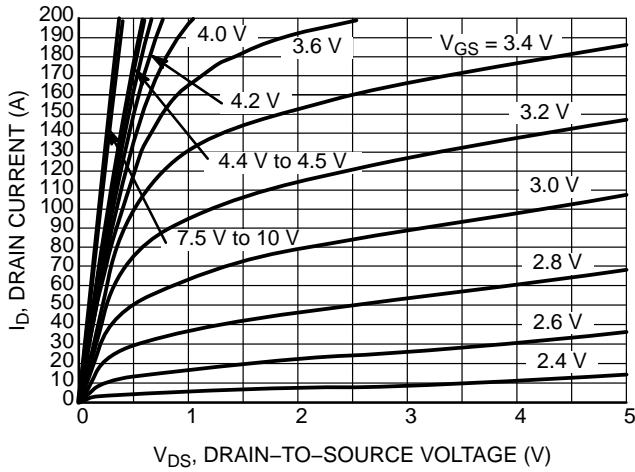


Figure 1. On-Region Characteristics

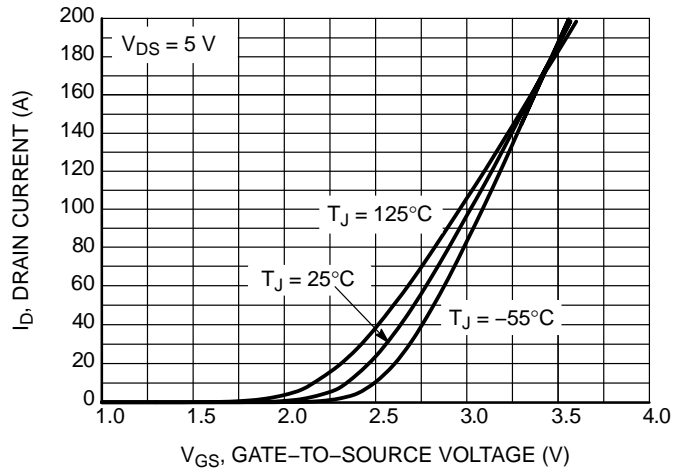


Figure 2. Transfer Characteristics

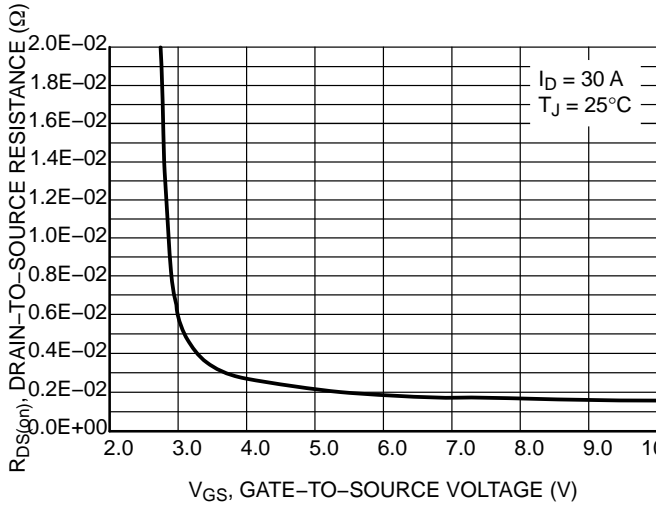


Figure 3. On-Resistance vs. Gate-to-Source Voltage

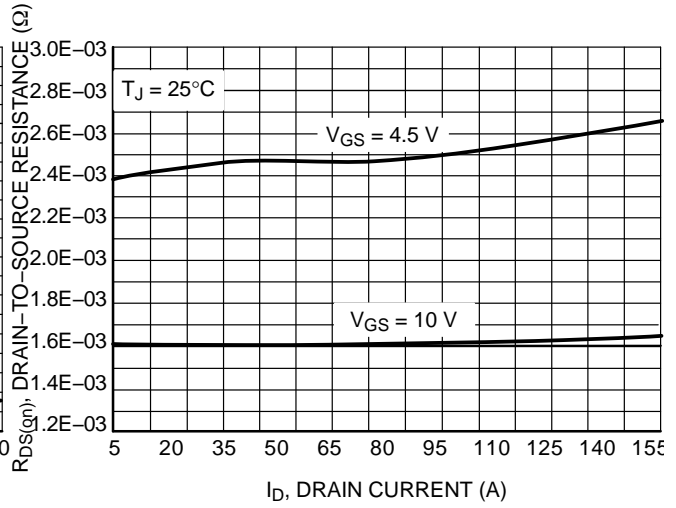


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

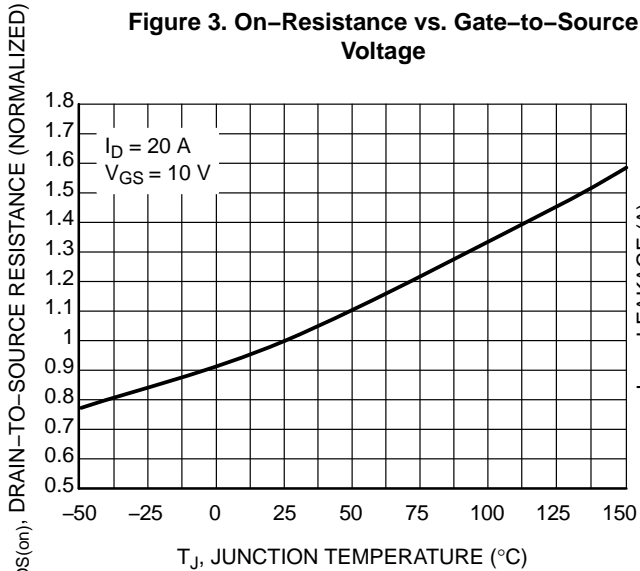


Figure 5. On-Resistance Variation with Temperature

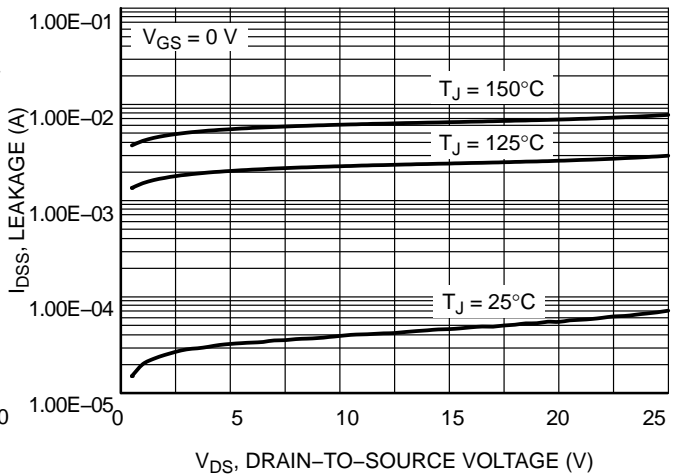


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

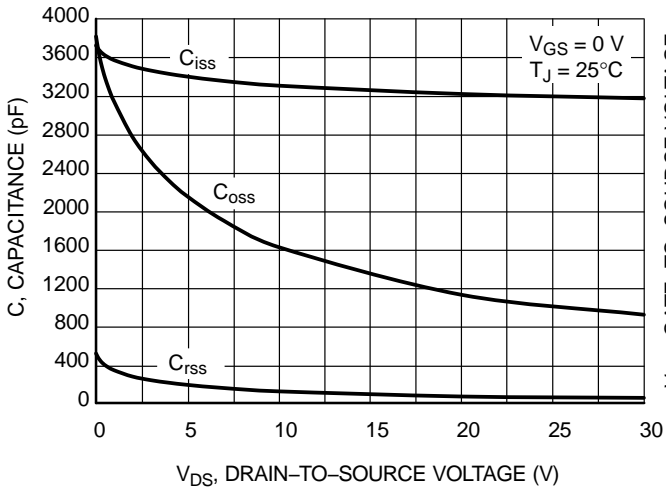


Figure 7. Capacitance Variation

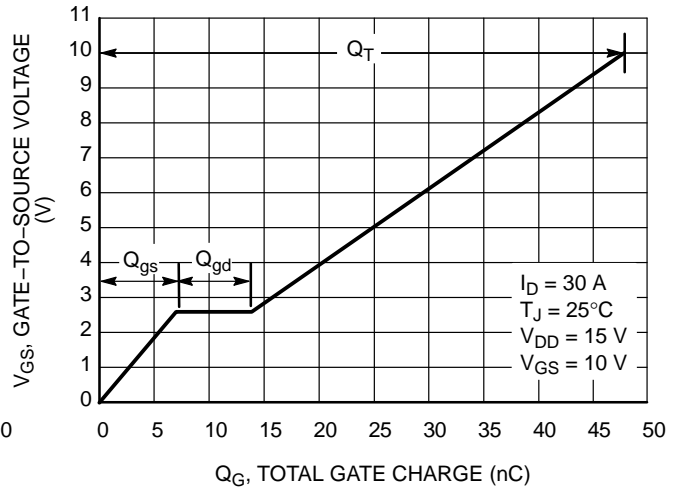


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

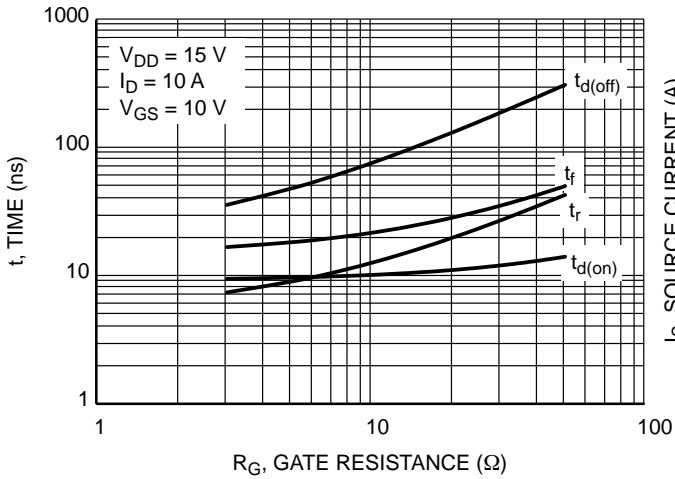


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

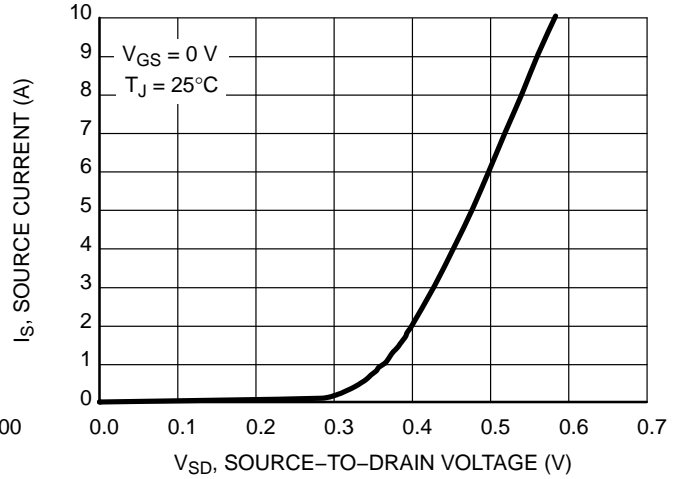


Figure 10. Diode Forward Voltage vs. Current

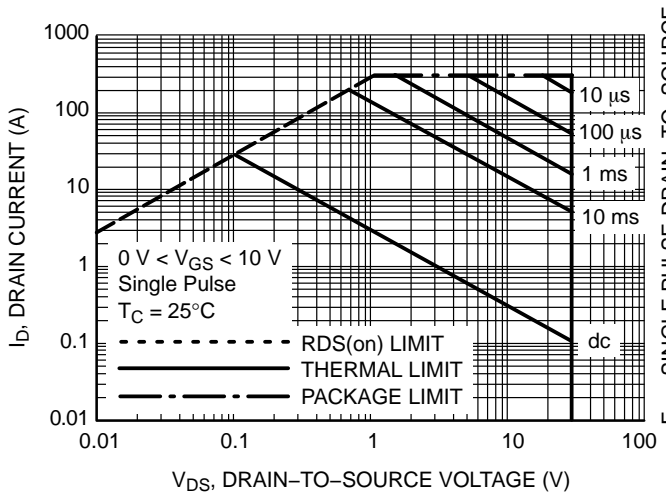


Figure 11. Maximum Rated Forward Biased Safe Operating Area

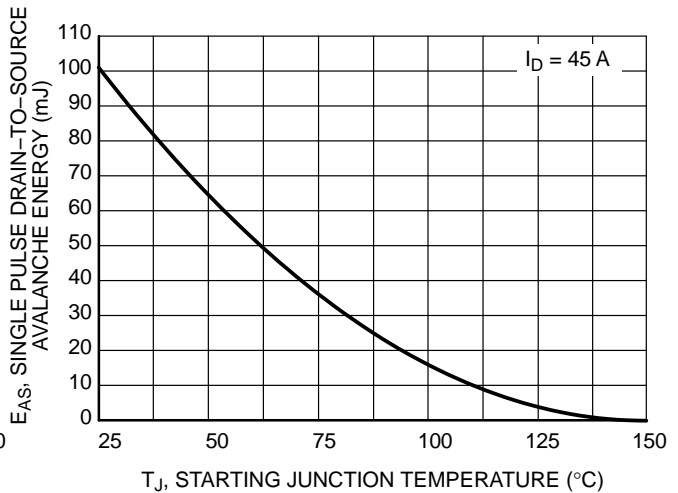


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTMFS4983NF

TYPICAL PERFORMANCE CURVES

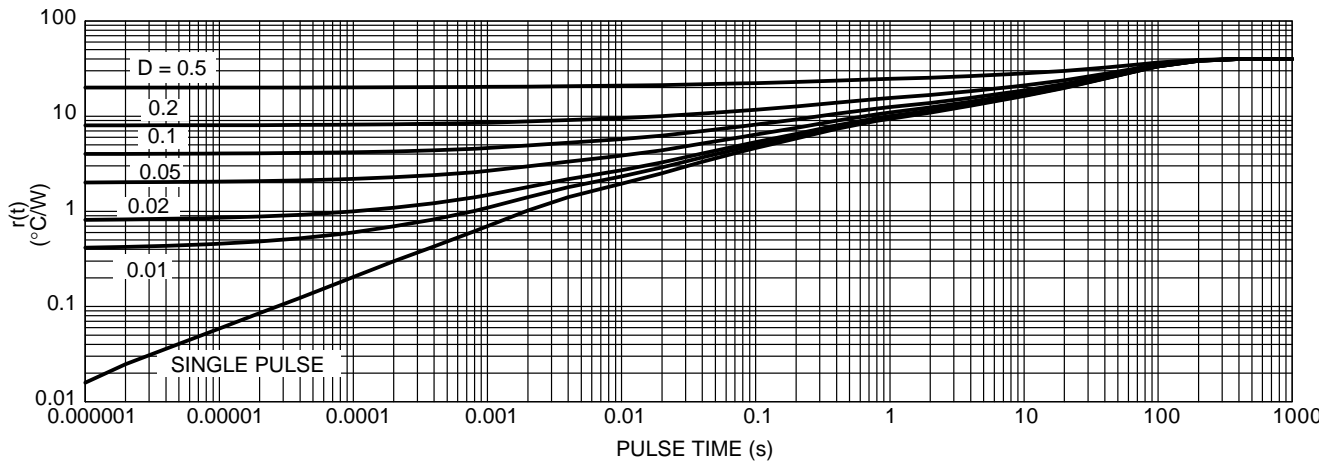


Figure 13. Thermal Response

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



1
SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

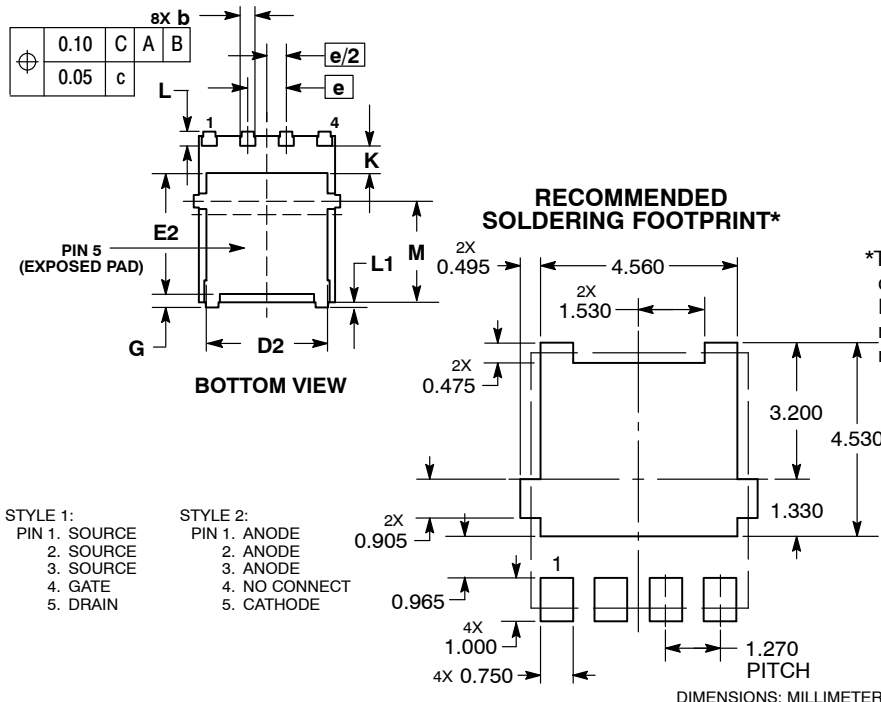
| DIM | MILLIMETERS | | |
|-----|-------------|-------|------|
| | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | --- | 0.05 |
| b | 0.33 | 0.41 | 0.51 |
| c | 0.23 | 0.28 | 0.33 |
| D | 5.00 | 5.15 | 5.30 |
| D1 | 4.70 | 4.90 | 5.10 |
| D2 | 3.80 | 4.00 | 4.20 |
| E | 6.00 | 6.15 | 6.30 |
| E1 | 5.70 | 5.90 | 6.10 |
| E2 | 3.45 | 3.65 | 3.85 |
| e | 1.27 BSC | | |
| G | 0.51 | 0.575 | 0.71 |
| K | 1.20 | 1.35 | 1.50 |
| L | 0.51 | 0.575 | 0.71 |
| L1 | 0.125 REF | | |
| M | 3.00 | 3.40 | 3.80 |
| θ | 0° | --- | 12° |

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|------------------|--------------------------|--|
| DOCUMENT NUMBER: | 98AON14036D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | DFN5 5x6, 1.27P (SO-8FL) | PAGE 1 OF 1 |

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales