

MOSFET - Power, Single **N-Channel, Logic Level, SO-8FL**

30 V, 1.7 mΩ, 159 A

NVMFS4C03N

Features

- Small Footprint (5x6 mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS4C03NWF Wettable Flanks Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	30	V
Gate-to-Source Voltage	9		V_{GS}	±20	٧
Continuous Drain Current R ₀ JC (Notes 2, 3, 4)	Steady State	T _C = 25°C	Ι _D	159	Α
Power Dissipation $R_{\theta JC}$ (Notes 2, 3)	Oldio	T _C = 25°C	P _D	77	W
Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3, 4)	Steady State	T _A = 25°C	I _D	34.9	Α
Power Dissipation $R_{\theta JA}$ (Notes 2, 3)	$T_A = 25^{\circ}C$		P _D	3.71	W
Pulsed Drain Current	$T_A = 25^\circ$	°C, t _p = 10 μs	I _{DM}	900	Α
Operating Junction and Storage Temperature			T _J , T _{stg}	–55 to 175	°C
Source Current (Body Diode)			I _S	64	Α
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 11 A)			E _{AS}	549	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C	

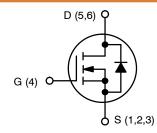
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 2)

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 3)	$R_{\theta JC}$	1.95	°C/W
Junction-to-Ambient - Steady State (Note 3)	$R_{\theta JA}$	40	

- 2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

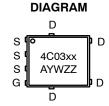
V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX
30 V	1.7 mΩ @ 10 V	159 A
30 V	2.4 mΩ @ 4.5 V	159 A



N-CHANNEL MOSFET







MARKING

SO-8 FL CASE 488AA

DFNW5 CASE 507BE

4C03N = Specific Device Code for NVMFS4C03N

4C03WF= Specific Device Code of NVMFS4C03NWF

= Assembly Location

= Year W = Work Week ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping [†]
NVMFS4C03NT1G	SO-8 FL (Pb-Free)	1500 / Tape & Reel
NVMFS4C03NWFT1G, NVMFS4C03NWFET1G	DFNW5 (Pb-Free)	1500 / Tape & Reel

DISCONTINUED (Note 1)

NVMFS4C03NT3G	SO-8 FL (Pb-Free)	5000 / Tape & Reel
NVMFS4C03NWFT3G	SO-8 FL (Pb-Free)	5000 / Tape & Reel

- †For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
- 1. DISCONTINUED: These devices are not recommended for new design. Please contact your onsemi representative for information. The most current information on these devices may be available on www.onsemi.com.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS						•	•
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA		30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /				18.2		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V,	T _J = 25 °C			1	
		V _{DS} = 24 V	T _J = 125°C			10	μΑ
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{G}$	_{iS} = 20 V			100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D = 250 \mu A$		1.3		2.2	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				4.8		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 30 A		1.4	1.7	_
		V _{GS} = 4.5 V	I _D = 30 A		2.0	2.4	mΩ
Forward Transconductance	9FS	V _{DS} = 3 V, I _D) = 30 A		136		S
Gate Resistance	R_{G}	T _A = 25 °C			1.0		Ω
CHARGES AND CAPACITANCES	•	•			•		•
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 15 V			3071		pF
Output Capacitance	C _{OSS}				1673		
Reverse Transfer Capacitance	C _{RSS}				67		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 15 V; I _D = 30 A			20.8		nC
Threshold Gate Charge	Q _{G(TH)}				4.9		
Gate-to-Source Charge	Q_{GS}				8.5		
Gate-to-Drain Charge	Q_{GD}				4.7		-
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 15 V, I _D = 30 A			45.2		nC
SWITCHING CHARACTERISTICS (Note 6)						1	
Turn-On Delay Time	t _{d(ON)}	V_{GS} = 4.5 V, V_{DS} = 15 V, I_{D} = 15 A, R_{G} = 3.0 Ω			14		
Rise Time	t _r				32		1
Turn-Off Delay Time	t _{d(OFF)}				27		ns ns
Fall Time	t _f				17		
DRAIN-SOURCE DIODE CHARACTERISTIC				1		ı	
Forward Diode Voltage	V_{SD}	V _{SD} V _{CO = 0 V}	T _J = 25°C		0.75	1.1	
		$V_{GS} = 0 V,$ $I_{S} = 10 A$	T _J = 125°C		0.6		V
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, } dI_{S}/dt = 100 \text{ A}/\mu\text{s,}$ $I_{S} = 30 \text{ A}$			47		
Charge Time	ta				23		ns
Discharge Time	t _b				24		†
Reverse Recovery Charge	Q _{RR}				39		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

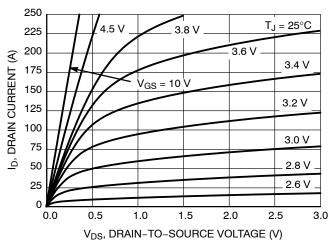
5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

250

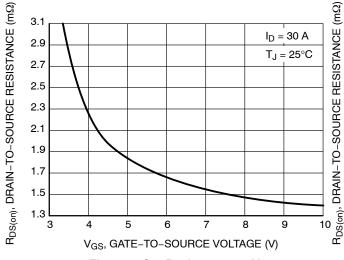
 $V_{DS} = 3 V$



225 200 ID, DRAIN CURRENT (A) 175 150 125 100 $T_{J} = 150^{\circ}C$ 75 50 -55°C 25 0 1.5 3.5 4.5 V_{GS}, GATE-TO-SOURCE VOLTAGE (V)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



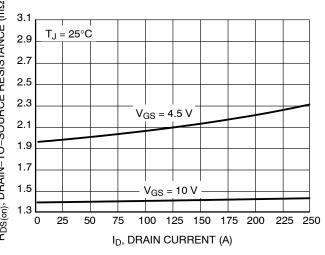
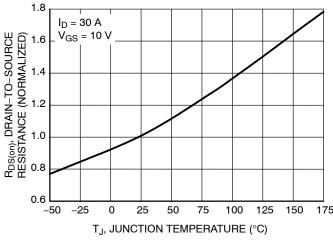


Figure 3. On-Resistance vs. V_{GS}

Figure 4. On-Resistance vs. Drain Current and Gate Voltage



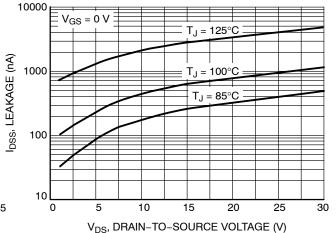


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

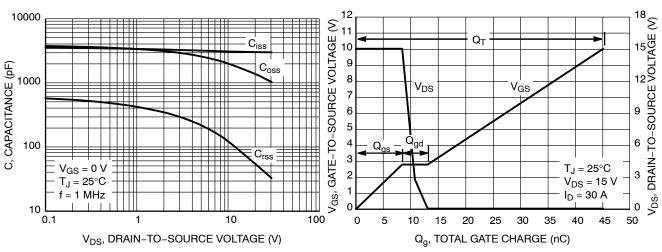


Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

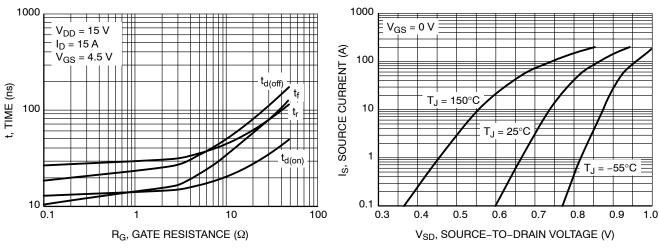


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current

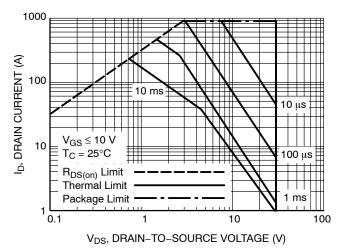


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

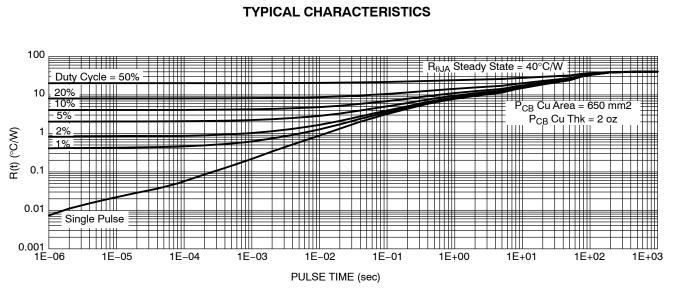


Figure 12. Thermal Impedance (Junction-to-Ambient)

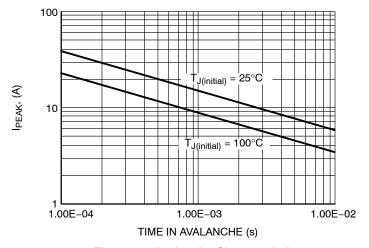


Figure 13. Avalanche Characteristics





0.10

SIDE VIEW

DFN5 5x6, 1.27P (SO-8FL) CASE 488AA ISSUE N

DATE 25 JUN 2018

NOTES:

- DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994. CONTROLLING DIMENSION: MILLIMETER. DIMENSION D1 AND E1 DO NOT INCLUDE
- MOLD FLASH PROTRUSIONS OR GATE BURRS

	MILLIMETERS					
DIM	MIN	NOM	MAX			
Α	0.90	1.00	1.10			
A1	0.00	-	0.05			
b	0.33	0.41	0.51			
С	0.23	0.28	0.33			
D	5.00	5.15	5.30			
D1	4.70	4.90	5.10			
D2	3.80	4.00	4.20			
E	6.00	6.15	6.30			
E1	5.70	5.90	6.10			
E2	3.45	3.65	3.85			
е	1.27 BSC					
G	0.51	0.575	0.71			
K	1.20	1.35	1.50			
L	0.51	0.575	0.71			
L1	0.125 REF					
M	3.00	3.40	3.80			
θ	0 °		12 °			

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code

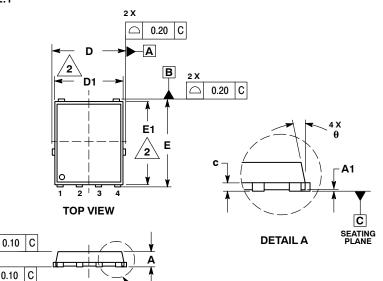
= Lot Traceability

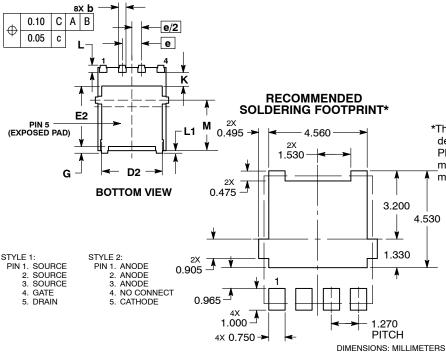
= Assembly Location Α

Υ = Year W = Work Week

ZZ

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ", may or may not be present. Some products may not follow the Generic Marking.





DETAIL A

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PIN 1

IDENTIFIER

// 0.10 C

□ 0.10 C

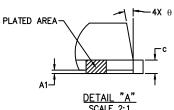
DFNW5 4.90x5.90x1.00, 1.27P

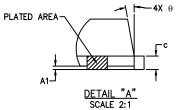
CASE 507BE **ISSUE A**

DATE 15 JUL 2024

NOTES:

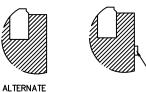
- DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-2018.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH. PROTRUSIONS, OR GATE BURRS.
- THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

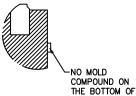






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TIE BAR.

MILLIMETERS DIM MIN NOM MAX Α 0.90 1.00 1.10 Α1 0.00 0.25 0.05 0.41 0.51 ь 0.33 0.33 0.23 С 0.28 D 5.00 5.15 5.30 D1 4.70 4.90 5.10 D2 3.80 4.00 4.20 Ε 6.00 6.15 6.30 E1 5.70 5.90 6.10 E2 3.45 3.65 3.85 E3 3.00 3.40 3.80 е 1.27 BSC 1.50 1.20 1.35 0.51 0.57 0.71 L2 0.15 REF 12° θ 0. 6*

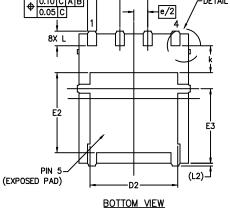
0.10 C A B DETAIL B CONSTRUCTION 0.05 C

TOP VIEW

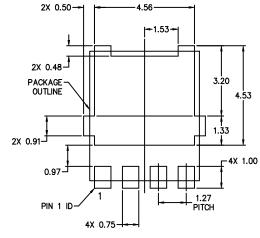
DETAIL A

SIDE VIEW

SEATING



DETAIL "B" SCALE 2:1



RECOMMENDED MOUNTING FOOTPRINT* *FOR ADDITIONAL INFORMATION ON OUR PD-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

GENERIC MARKING DIAGRAM*



= Assembly Location Α Υ = Year

W = Work Week 77 = Lot Traceability

XXXXXX = Specific Device Code *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION: DFNW5 4.90x5.90x1.00, 1.27P **PAGE 1 OF 1**

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