

MOSFET – Power, Single N-Channel

60 V, 250 A, 1.36 mΩ

NVMFS5C612NL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5C612NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit	
V_{DSS}	Drain-to-Source Voltage	60	V	
V_{GS}	Gate-to-Source Voltage	± 20	V	
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State		
		$T_C = 25^\circ\text{C}$	250	A
P_D	Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State		
		$T_C = 100^\circ\text{C}$	175	W
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State		
		$T_A = 25^\circ\text{C}$	38	A
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	Steady State		
		$T_A = 100^\circ\text{C}$	27	W
I_{DM}	Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	900	A
T_J, T_{stg}	Operating Junction and Storage Temperature	-55 to +175	$^\circ\text{C}$	
I_S	Source Current (Body Diode)	164	A	
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 17 \text{ A}$)	451	mJ	
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	260	$^\circ\text{C}$	

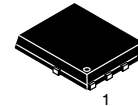
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

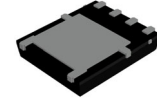
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State	0.9	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

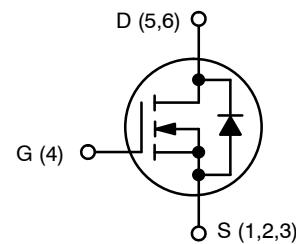
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
60 V	1.36 mΩ @ 10 V	250 A
	2.3 mΩ @ 4.5 V	



DFN5
(SO-8FL)
CASE 488AA
STYLE 1

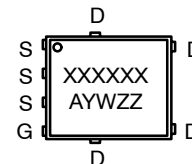


DFNW5
CASE 507BE



N-CHANNEL MOSFET

MARKING DIAGRAM



XXXXXX = 5C612L
(NVMFS5C612NL) or
612LWF
(NVMFS5C612NLWF)

A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been DISCONTINUED. Please refer to the table on page 5.

NVMFS5C612NL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient			12.7		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25\ ^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		250	
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 4)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.2		2.0	V
$V_{GS(TH)}/T_J$	Threshold Temperature Coefficient			-5.76		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		1.13	1.36	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 50\text{ A}$		1.65	2.3	
g_{FS}	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 50\text{ A}$		151		S

CHARGES, CAPACITANCES & GATE RESISTANCE

C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 25\text{ V}$		6660		pF
C_{OSS}	Output Capacitance			2953		
C_{RSS}	Reverse Transfer Capacitance			45		
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$		41		nC
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$		91		
$Q_{G(TH)}$	Threshold Gate Charge	$V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$		5		
Q_{GS}	Gate-to-Source Charge			17.1		
Q_{GD}	Gate-to-Drain Charge			10.9		
V_{GP}	Plateau Voltage			2.9		V

SWITCHING CHARACTERISTICS (Note 5)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}, I_D = 50\text{ A}, R_G = 1.0\ \Omega$		19		ns
t_r	Rise Time			51		
$t_{d(OFF)}$	Turn-Off Delay Time			47		
t_f	Fall Time			18		

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$	$T_J = 25^\circ\text{C}$		0.78	1.2	V
			$T_J = 125^\circ\text{C}$		0.66		
t_{RR}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 50\text{ A}$		78		ns	
t_a	Charge Time			36			
t_b	Discharge Time			42			
Q_{RR}	Reverse Recovery Charge			105			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

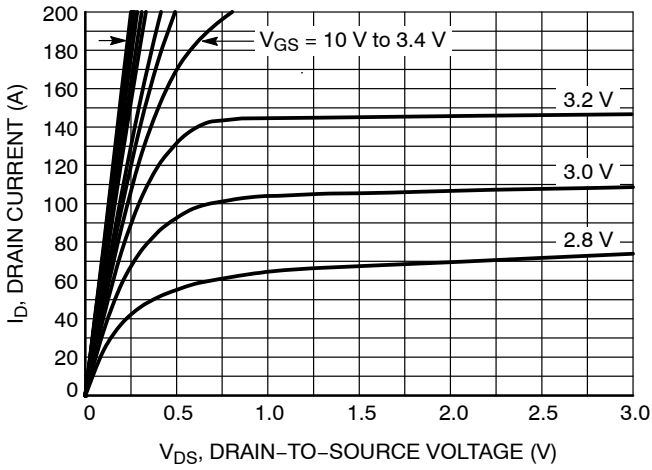


Figure 1. On-Region Characteristics

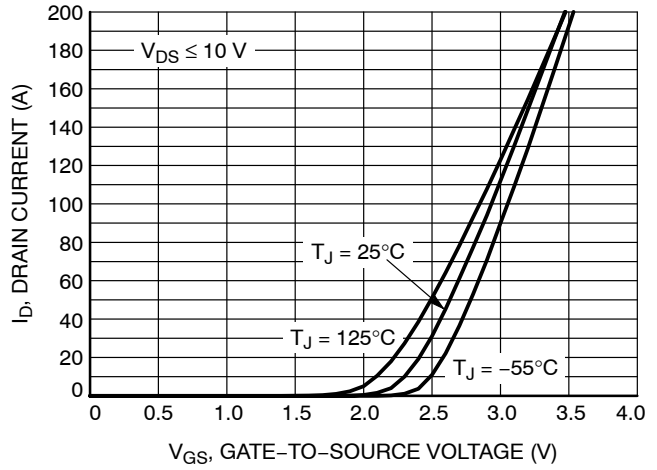


Figure 2. Transfer Characteristics

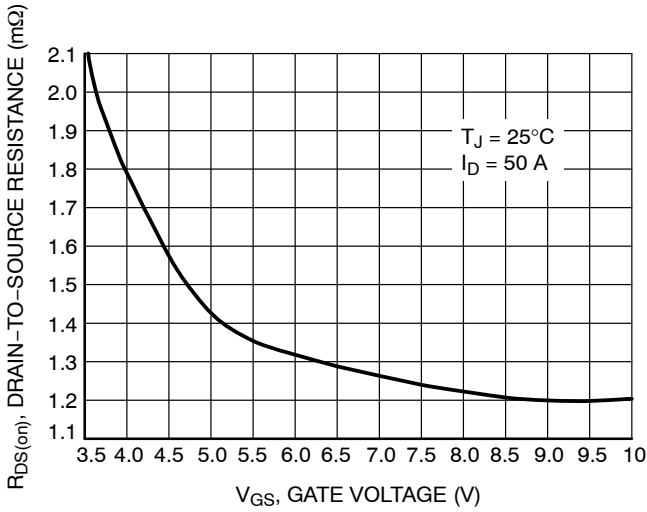


Figure 3. On-Resistance vs. Gate-to-Source Voltage

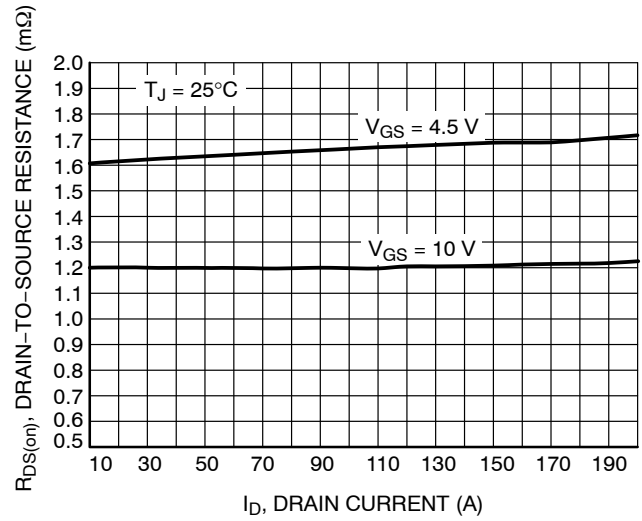


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

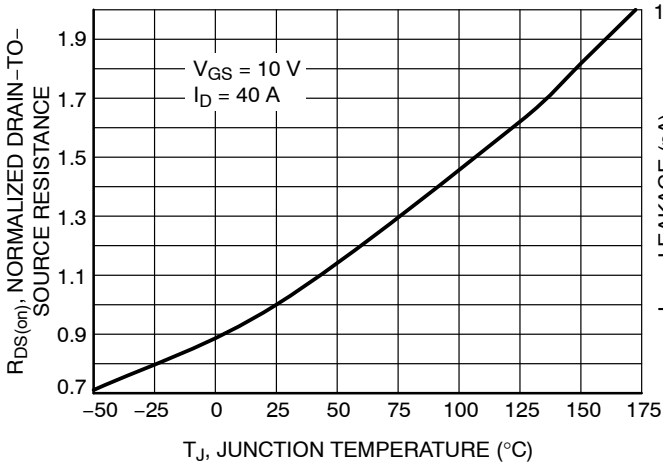


Figure 5. On-Resistance Variation with Temperature

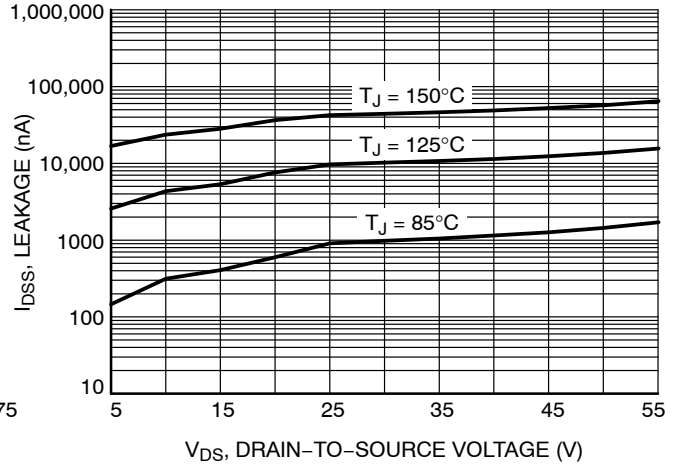


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NVMFS5C612NL

TYPICAL CHARACTERISTICS (continued)

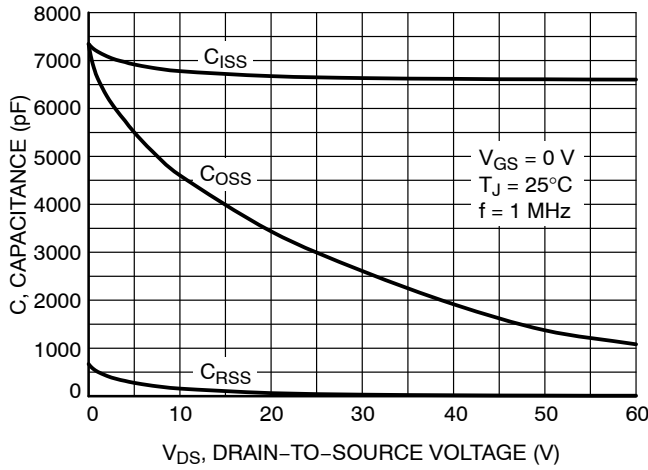


Figure 7. Capacitance Variation

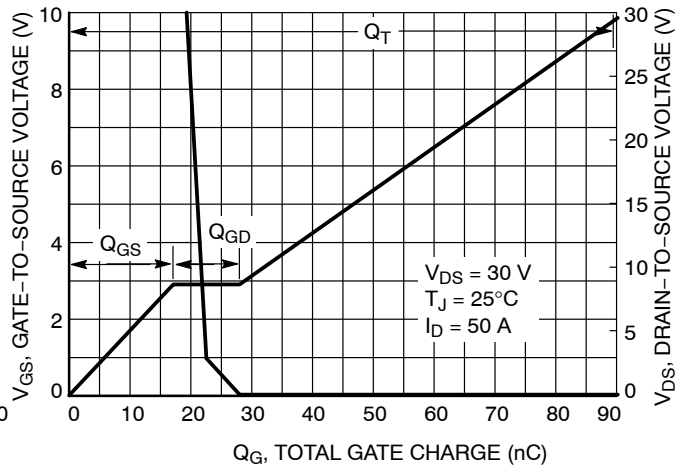


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

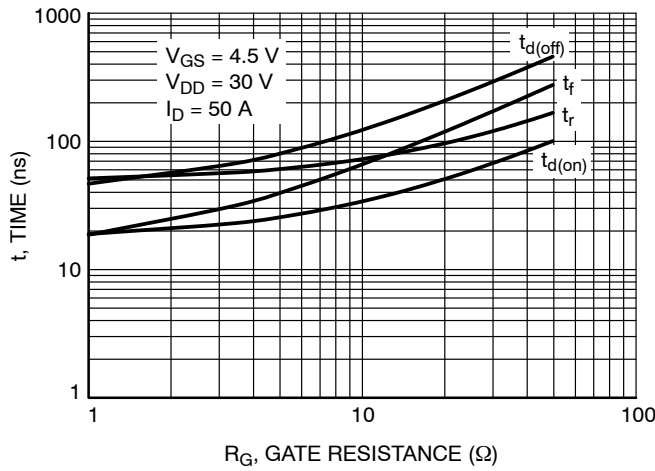


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

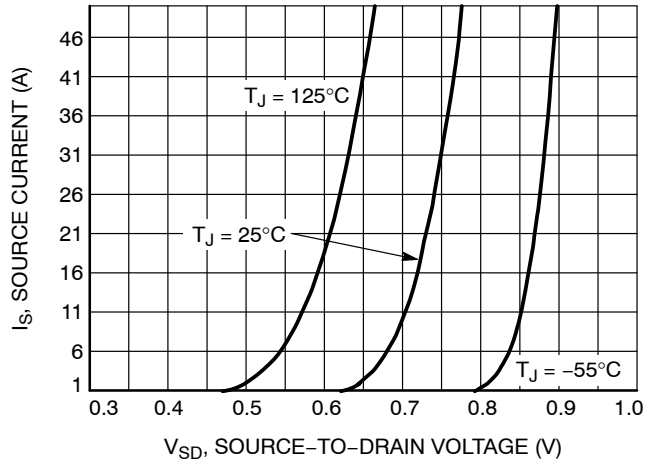


Figure 10. Diode Forward Voltage vs. Current

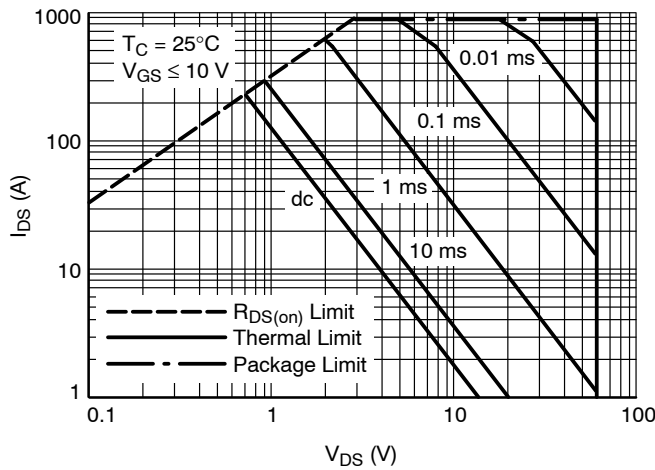


Figure 11. Safe Operating Area

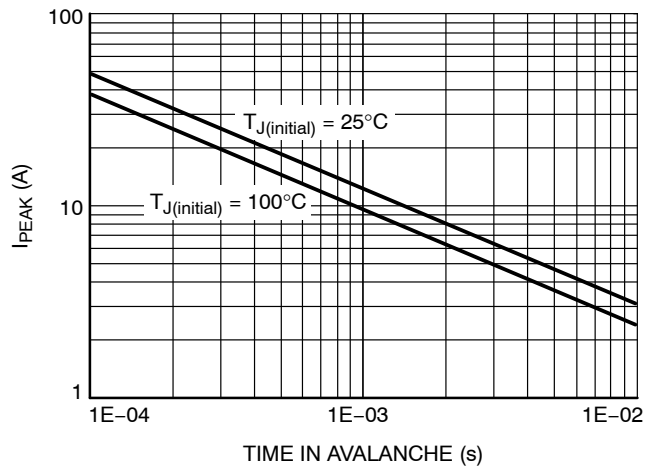


Figure 12. I_{PEAK} vs. Time in Avalanche

NVMFS5C612NL

TYPICAL CHARACTERISTICS (continued)

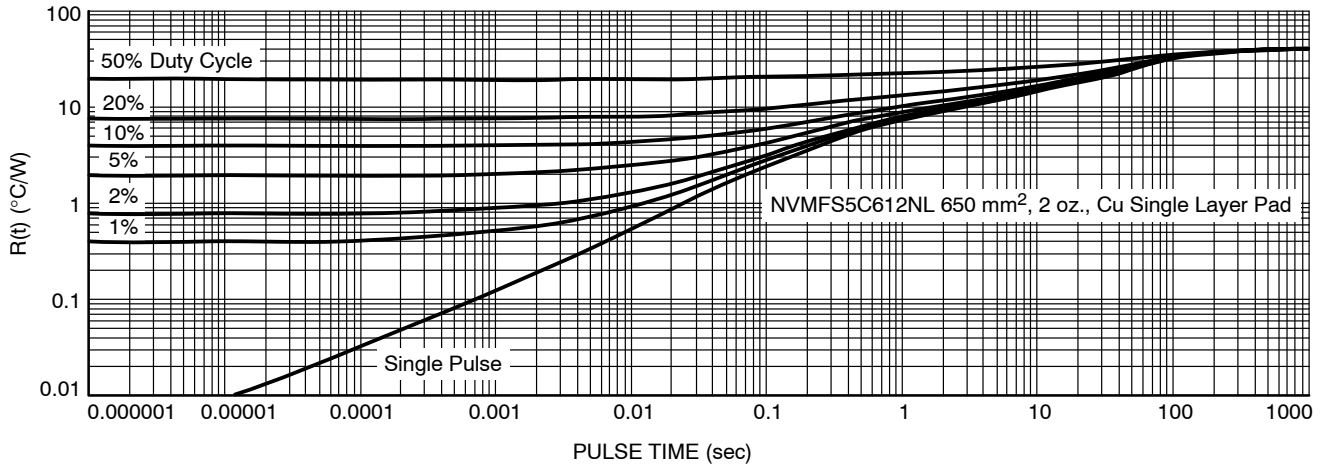


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMFS5C612NLT1G	5C612L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C612NLWFT1G	612LWF	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C612NLAFT1G	5C612L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C612NLWFAFT1G	612LWF	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

DISCONTINUED (Note 6)

NVMFS5C612NLT3G	5C612L	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS5C612NLWFT3G	612LWF	DFN5 (Pb-Free, Wettable Flanks)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

6. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



1
SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



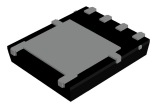
- STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
- STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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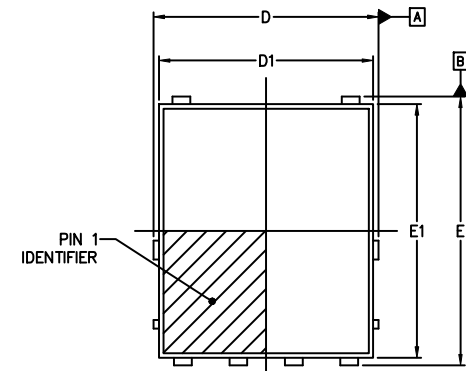


DFNW5 4.90x5.90x1.00, 1.27P
CASE 507BE
ISSUE A

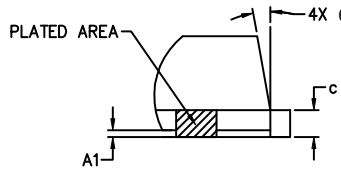
DATE 15 JUL 2024

NOTES:

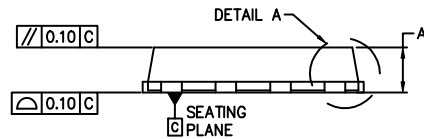
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.



TOP VIEW



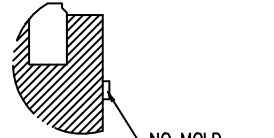
DETAIL "A"
SCALE 2:1



SIDE VIEW

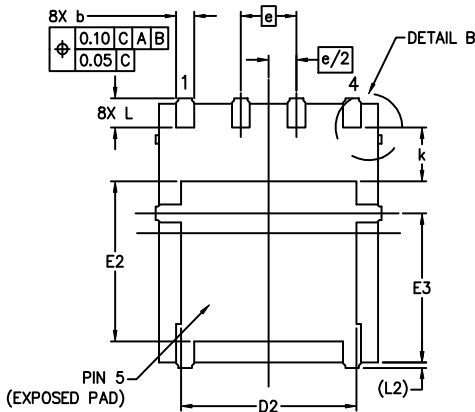


ALTERNATE CONSTRUCTION



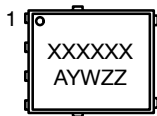
DETAIL "B"
SCALE 2:1

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	0.25	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
θ	0°	6°	12°

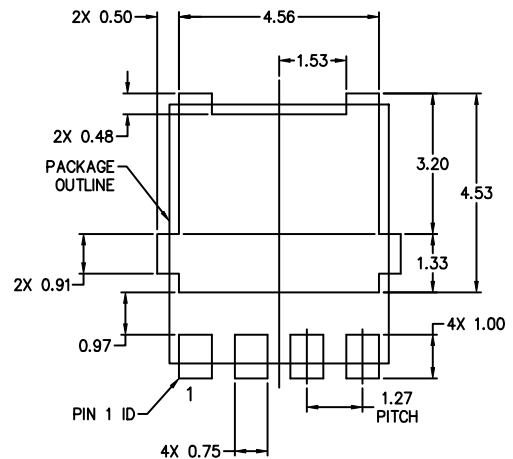


BOTTOM VIEW

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability
- *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*
 *FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	DFNW5 4.90x5.90x1.00, 1.27P	PAGE 1 OF 1

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