

MOSFET – Power, Single N-Channel, DFN5/DFNW5

60 V, 250 A, 1.3 mΩ

NVMFS5H600NL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Value	Unit	
V_{DSS}	Drain-to-Source Voltage		60	V	
V_{GS}	Gate-to-Source Voltage		± 20	V	
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	250	A
			$T_C = 100^\circ\text{C}$	160	
P_D	Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	160	W
			$T_C = 100^\circ\text{C}$	63	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	35	A
			$T_A = 100^\circ\text{C}$	22	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	3.3	W
			$T_A = 100^\circ\text{C}$	1.3	
I_{DM}	Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	900	A	
T_J, T_{stg}	Operating Junction and Storage Temperature		-55 to +175	$^\circ\text{C}$	
I_S	Source Current (Body Diode)		170	A	
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 26 \text{ A}$)		338	mJ	
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		260	$^\circ\text{C}$	

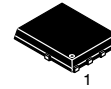
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

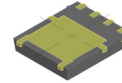
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State	0.80	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	38	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
60 V	1.3 mΩ @ 10 V	250 A
	1.7 mΩ @ 4.5 V	

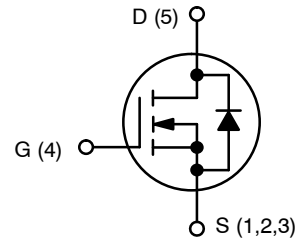


DFN5
CASE 506EZ

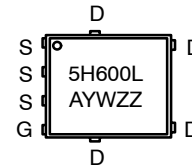


DFNW5
CASE 507BA

N-CHANNEL MOSFET



MARKING DIAGRAM



5H600L = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

NVMFS5H600NL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient			34.3		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		250	
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 4)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.2		2.0	V
$V_{GS(TH)}/T_J$	Threshold Temperature Coefficient			-5.0		mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}$	$I_D = 50\text{ A}$	1.1	1.3	m Ω
		$V_{GS} = 4.5\text{ V}$	$I_D = 50\text{ A}$	1.4	1.7	
g_{FS}	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 50\text{ A}$		280		S

CHARGES, CAPACITANCES & GATE RESISTANCE

C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 30\text{ V}$		6680		pF
C_{OSS}	Output Capacitance			1230		
C_{RSS}	Reverse Transfer Capacitance			30		
Q_{OSS}	Output Charge	$V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}$		100		nC
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$		40		
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$		89		
$Q_{G(TH)}$	Threshold Gate Charge	$V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$		11		
Q_{GS}	Gate-to-Source Charge			20		
Q_{GD}	Gate-to-Drain Charge			6.5		
V_{GP}	Plateau Voltage			3.0		V

SWITCHING CHARACTERISTICS (Note 5)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}, I_D = 50\text{ A}, R_G = 2.5\ \Omega$		28		ns
t_r	Rise Time			130		
$t_{d(OFF)}$	Turn-Off Delay Time			88		
t_f	Fall Time			160		

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$	$T_J = 25^\circ\text{C}$		0.77	1.2	V
			$T_J = 125^\circ\text{C}$		0.63		
t_{RR}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 50\text{ A}$		72		ns	
t_a	Charge Time			36			
t_b	Discharge Time			36			
Q_{RR}	Reverse Recovery Charge			60		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

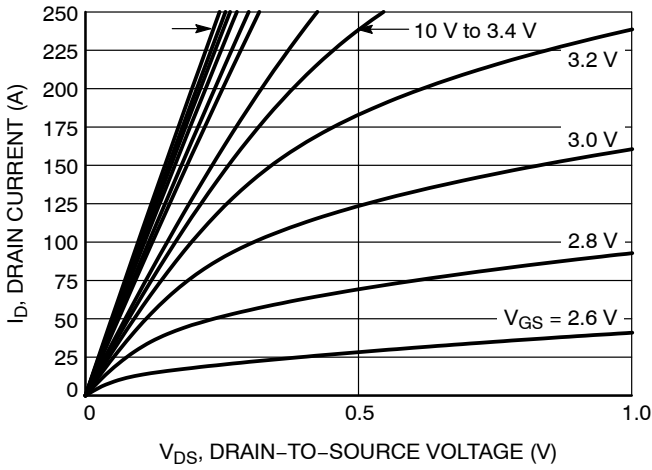


Figure 1. On-Region Characteristics

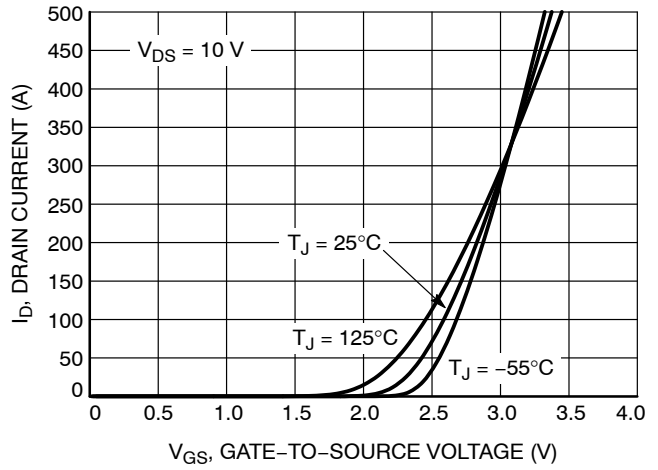


Figure 2. Transfer Characteristics

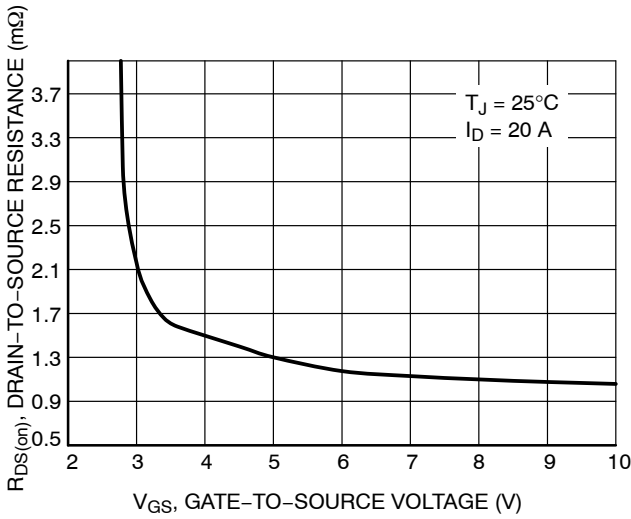


Figure 3. On-Resistance vs. Gate-to-Source Voltage

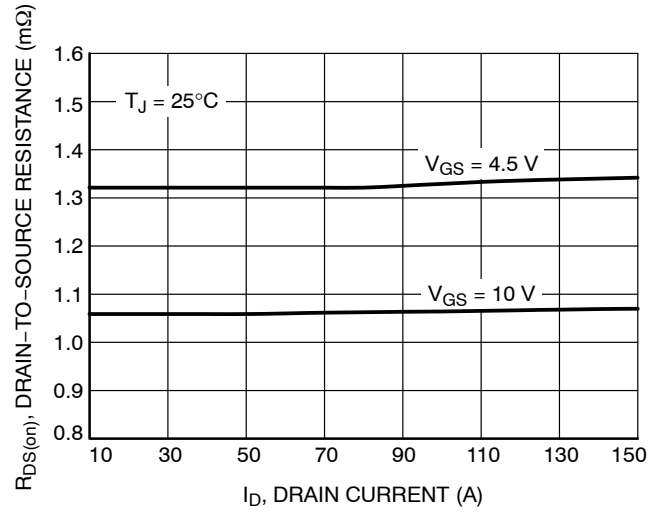


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

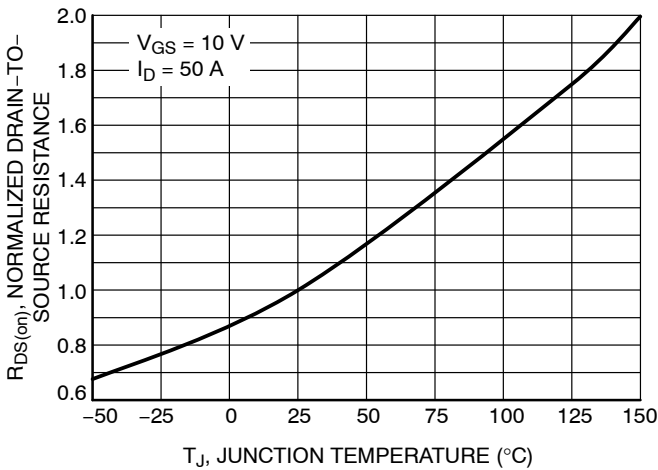


Figure 5. On-Resistance Variation with Temperature

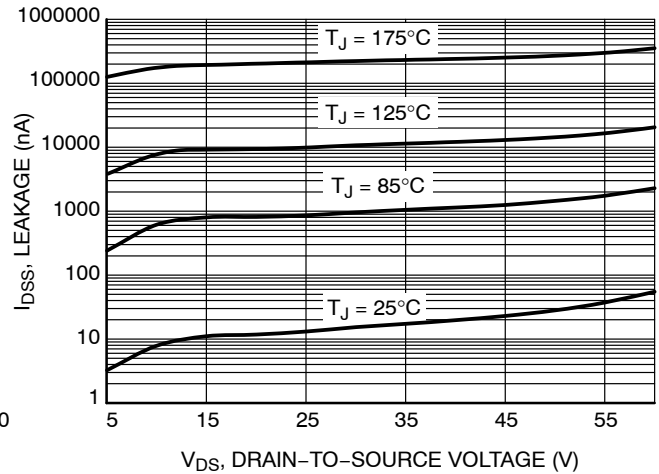


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS (continued)

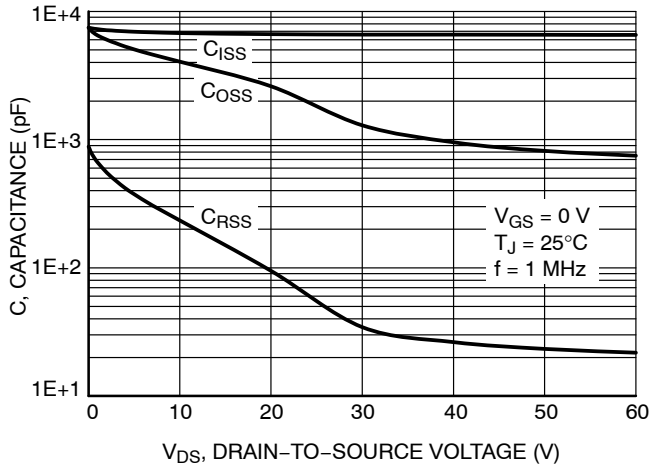


Figure 7. Capacitance Variation

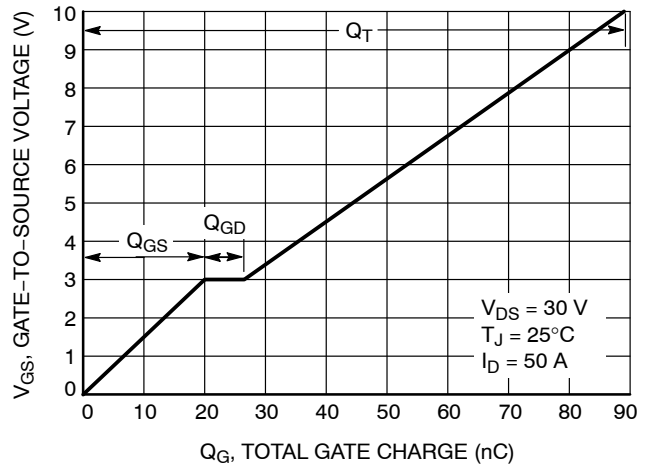


Figure 8. Gate-to-Source Voltage vs. Total Charge

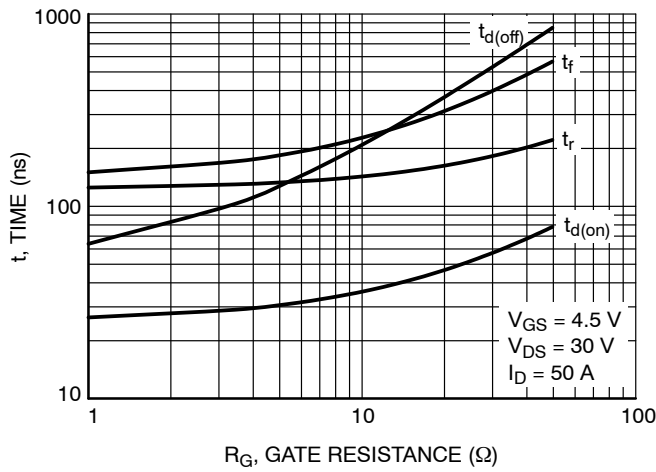


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

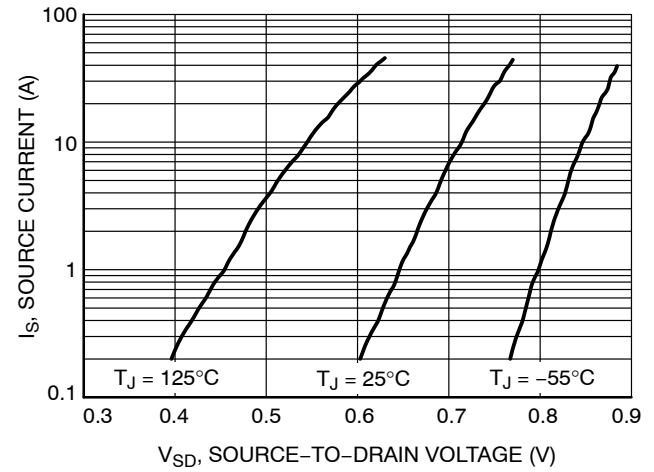


Figure 10. Diode Forward Voltage vs. Current

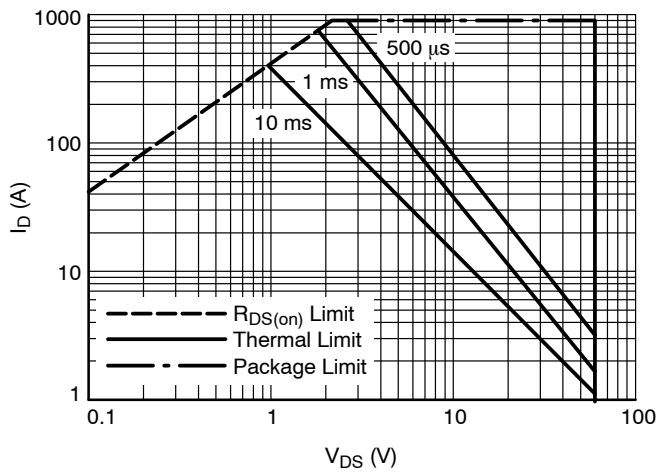


Figure 11. Safe Operating Area

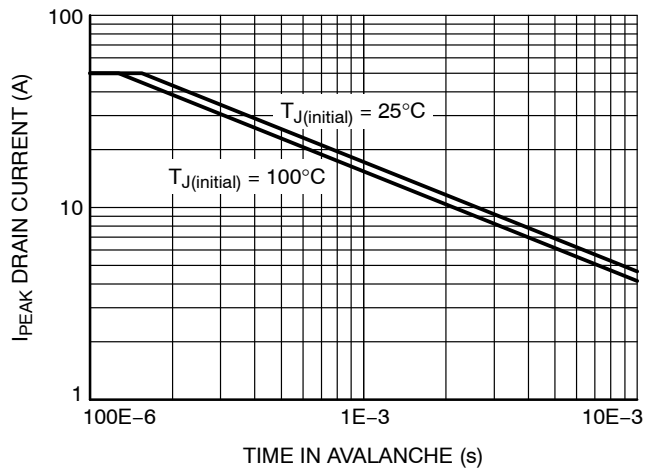


Figure 12. IPEAK vs. Time in Avalanche

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TYPICAL CHARACTERISTICS (continued)

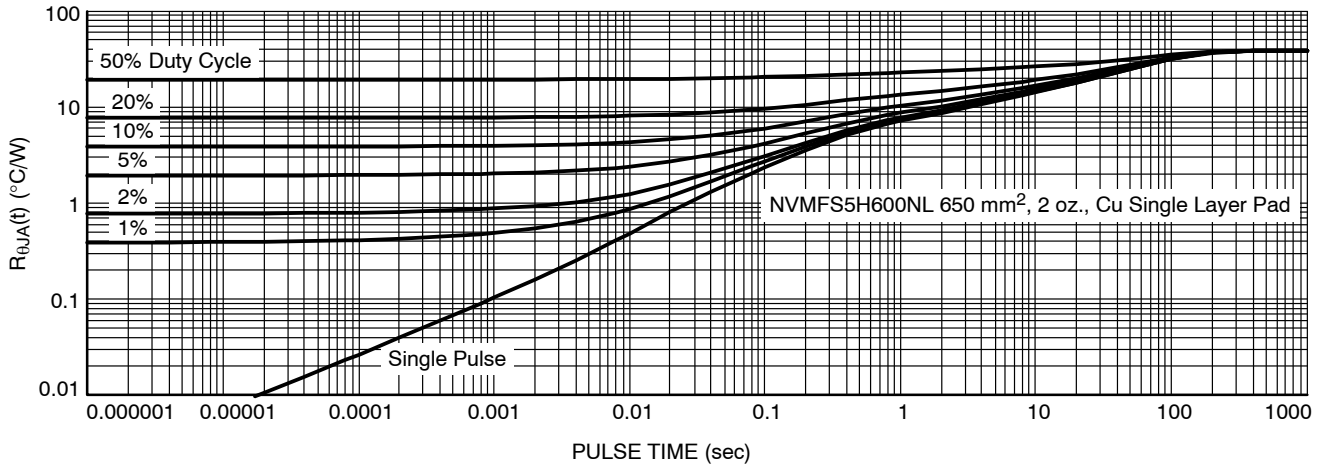


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Case	Marking	Package	Shipping†
NVMFS5H600NLT1G	506EZ	5H600L	DFN5 (Pb-Free)	1500 / Tape & Reel

DISCONTINUED (Note 6)

NVMFS5H600NLT3G	506EZ	5H600L	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS5H600NLWFT1G	507BA	600LWF	DFNW5 (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

6. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

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