ES_QN908x

Errata sheet QN908x

Rev. 1.1 — 23 February 2018 **Errata sheet**

Document information

Info	Content
Keywords	QN908x, errata
Abstract	QN908x errata

Revision history

Rev	Date	Description
00.01	20160809	Initial draft
00.02	20160901	Reviewed internally and updated
00.03	20161125	Removed some issue after Metal fix
00.04	20170307	Change document name and version
00.06	20170427	Update from v00.04, add RTC in errata, change TSC name into CS
1.0	20170601	Change document revision number to 1.0
1.1	20180223	ESD issue fixed

Contact information

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1. Introduction

This document describes QN908x errata which should be referred by customer while application development.

2. Product Identification

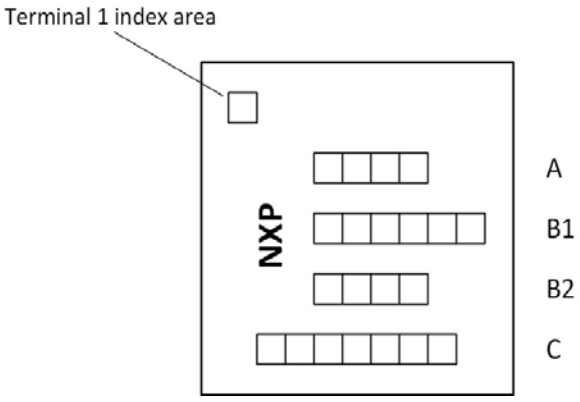

Figure 1 HVQFN48 package marking

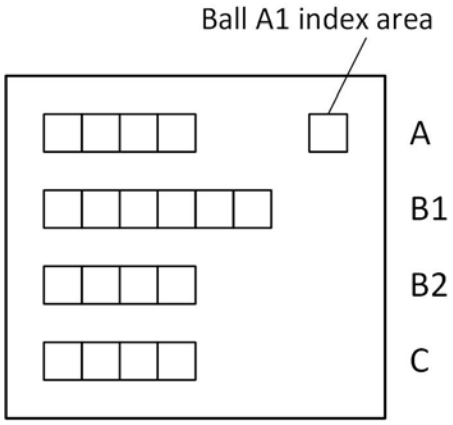

Figure 2 WLCSP47 package marking

The QN9080 HVQFN package has the following top-side marking:

- Line A: “9080” for QN9080
- Line B1: xxxxxx
- Line B2: xxxx
- Line C: xxYYWW[R]
  - YY: year code, 16 for 2016.
  - WW: week code.
  - R = Chip revision.

The QN9083 WLCSP package has the following top-side marking:

- Line A: “9083” for QN9083
- Line B1: xxxxxx

- Line B2: xxWW
  - WW: week code.
- Line C: YY[R]x
  - YY: year code, 16 for 2016.
  - R = Chip revision.

Table 1. Revision overview table

Revision identifier	Revision description
'A'	Initial device revision
'B'	First metal fix revision
'C'	Second metal fix revision
'D'	ESD problem fixed

3. Errata Overview

Table 2. Errata summary table

Erratum ID	Short description	Product version(s)	Detailed description
FSP.1	FIR coefficient can only be saved in low 64K SRAM	'A', 'B', 'C', and 'D'	Section 4.1
FC.1	Flexcomm (0~3) interrupt can't be wakeup source in sleep mode if SLEEPDEEP bit of Cortex-M4 SCR register is 1	'A', 'B', 'C', and 'D'	Section 4.2
FC.2	TXIDLE bit error in USART synchronous slave mode	'A', 'B', 'C', and 'D'	Section 4.3
COMPARATOR.1	Comparator can't work correctly under some condition	'A', 'B', 'C', and 'D'	Section 4.4
COMPARATOR.2	Comparator can't work correctly under some condition	'A', 'B', 'C', and 'D'	Section 4.5
CS.1	SCAN_INTEN register cannot be read	'A', 'B', 'C', and 'D'	Section 4.6
RTC.1	SEC, CNT_VAL and CNT2 register reading may return invalid values when happens at 32k clock positive edge	'A', 'B', 'C', and 'D'	Section 4.7
ESD.1	DCDC does not meet the required 2 kV ESD HBM specification	'A', 'B', and 'C'	Section 4.8

4. Errata Details

4.1 FSP.1: FIR coefficients can only be stored in low 64K SRAM

Introduction:

FIR coefficients can be stored anywhere in the 128K SRAM, and FIR engine will read it for computation.

Problem:

The FIR coefficient base address register (FIR_CH<x>_COEF_BASE, x = 0-8) is only 16 bit, which means only 64K SRAM is accessible. If the FIR coefficient is saved in high 64K, FIR can't fetch it.

Work-arounds:

Coefficient can only be stored in low 64K SRAM.

4.2 FC.1: Flexcomm (0~3) interrupt can't be wakeup source in sleep mode if SLEEPDEEP bit of Cortex-M4 SCR register is 1

Introduction:

Flexcomm (0~3) interrupt should be a wakeup source in sleep mode, no matter what value the SLEEPDEEP bit of Cortex-M4 System Control Register (SCR) is.

Problem:

Flexcomm (0-3) can't wake up MCU from sleep mode if the SLEEPDEEP bit in SCR is 1.

Work-arounds:

If Flexcomm are used as wakeup source, set SLEEPDEEP bit as 0 in sleep mode. The power saving from SLEEPDEEP=1 is negligible.

4.3 FC.2: TXIDLE bit error in USART synchronous slave mode

Introduction:

TXIDLE bit in USART Status register (STAT) should be 1 after transmit is finished in synchronous slave mode.

Problem:

When USART works in synchronous slave mode, TXIDLE bit in USART Status register (STAT) is set one cycle after transmit completes. The TXIDLE signal is not asserted correctly if the synchronous CLK from USART master doesn't provide that extra clock cycle.

Work-arounds:

Ignore the TXIDLE bit in synchronous slave mode. Use the buffer status as the indication of transmit completion.

4.4 COMPARATOR.1: Comparator cannot work correctly under some condition

Introduction:

Comparator should work well when internal reference is VCC*(15/16).

Problem:

When VCC<=1.8V and one of the analog comparator input is selected as internal reference=VCC*(15/16), the analog comparator does not function correctly. The analog comparator result does not change to logic “1” even if another input is >VCC*(15/16).

Work-arounds:

No work-arounds.

4.5 COMPARATOR.2: Comparator cannot work correctly under some condition

Introduction:

Comparator should work well when internal reference is (1/16)*VCC.

Problem:

When VCC<=1.8V and one of the analog comparator input is selected as internal reference=VCC*(1/16), the analog comparator does not function correctly. The analog comparator result does not change to logic “1” even if another input is >VCC*(1/16).

Work-arounds:

No work-arounds.

4.6 CS.1: SCAN_INTEN register cannot be read back correctly

Introduction:

SCAN_INTEN register, bit 3 in address 0x4000780C should be RMW correctly.

Problem:

SCAN_INTEN register, bit 3 in address 0x4000780C can’t be read by MCU.

This bit will always read back 0. If read-modify-write is used to modify this register, this bit will be written as 0.

Work-arounds:

Software should keep track of this register value. Always modify on the software saved value rather than read-back value when changing this register.

4.7 RTC.1: SEC, CNT_VAL, CNT2 register read return invalid value

Introduction:

Reading SEC, CNT_VAL and CNT2 registers, may return invalid values when it happens at the edge of 32K clock.

Problem:

These registers are 32k domain register, and they are mapping to APB clock domain. There is only a stage of synchronization of these registers. So when the reading operation happens at the edge of the 32K clock, the reading back value may be invalid.

Work-arounds:

Software need to read more times, when get 2 same value. It should be the correct one.

4.8 ESD.1: DCDC does not meet the required 2 kV ESD HBM specification

Introduction:

The chip is rated for 2 kV ESD HBM. ESD HBM stressed as highlighted a weakness in the DCDC IP.

Problem:

DCDC IP is passing ESD-HBM stress at 500V and failing above. When stressing the device with a level above 500V, DCDC IP will be damaged but the device is fully functional when the DCDC is using external power supplies.

Work-arounds:

This problem is fixed in Rev. D.

For the earlier reversions, it is not recommended to enable the DCDC. In such case, make sure to connect the VCC/VVD1/VDD2/VDD3 pins all together.

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