Application Note

ZDP14x0P128D

Chip for image display application

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Overview

The ZDP14x0 series is a series of image display specific driver chips developed by Guangzhou Zhiyuan Microelectronics based on the AWTK GUI engine. Maximum internal integrated 64MB display memory, 2D graphics accelerator, MJPEG decoding, audio decoder and other rich multimedia functions. It has two display interfaces, RGB/MIPI, and supports a maximum screen resolution of 1920 * 1080. Supports SPI/UART communication with external controllers and multiple UI firmware upgrade modes.

Features

- Built in AWTK GUI engine, paired with AWTK Designer upper computer drag and drop development
- Built in 64MB/16MB display memory;
- Built in image processor, supports 2D graphics acceleration, rotation, scaling, and supports alpha blend;
- Built in audio decoding, audio playback;
- Support RGB and MIPI interface LCD screens;
- The maximum resolution supports 1920 * 1080;
- Support screen resistance touch and capacitor touch options;
- Supports backlight adjustment and can be equipped with PWM frequency and duty cycle;
- Supporting 1 communication serial port (supporting flow control), SPI slave;
- Support SPI flash interface, NOR and NAND, with configurable capacity;
- Support USB download, USB and SD card upgrades;

Application

- Serial port screen
- Advertising machine
- Attendance machine
- Video door entry system

Ordering information

Part number	Graphics memory	Package type
ZDP1440P128D	16MB	LQFP128
ZDP1460P128D	64MB	LQFP128

Revision history

version	date	cause
1.0.00	2022/07/18	Create this document

目 录

1. Introduction 1
1.1 Overview 1
1.2 Features 1
1.3 specification 2
2. Signals and Connections 3
2.1 Pin Definitions 3
3. Electrical Specifications 3-1
3.1 Maximum Ratings 3-1
3.2 Recommended Operating Range 3-1
3.3 Electrical Characteristics of PMU 3-1
3.4 DC Electrical Characteristics 3-2
3.5 AC Electrical Characteristics 3-2
4. Typical application circuits 4-4
4.1 Power 4-4
4.2 PMU 4-4
4.2.1 PMU internal structure 4-4
4.2.2 PMU 4-5
4.2.3 Voltage Range Parameters 4-5
4.3 System module power pins 4-5
4.3.1 VDD_DDR 和 VREF_DDR 4-5
4.4 Clock 4-6
4.4.1 24MHz crystal oscillator circuit 4-6
4.4.2 32.768KHz 晶振电路 4-6
4.5 RESET 4-6
4.6 BOOT 4-6
4.7 SPI flash 4-7
4.8 USB 4-7
4.9 SD card interface 4-7
4.10 LCD 4-8
4.10.1 MIPI interfaces 4-8
4.10.2 RGB Interface 4-8
4.11 Communication Interface 4-9
4.12 Touch interface 4-9
4.13 Others 4-9
5. Package Information 5-10
6. Reflow Profile 1
7. Storage and Baking 2
8. Disclaimer 3

1. Introduction

1.1 Overview

The ZDP14x series is a series of image display specific driver chips developed by Guangzhou Zhiyuan Microelectronics based on the AWTK GUI engine. Internally integrated with a maximum of 64MB of display memory, 2D graphics accelerator, MJPEG decoder, audio decoder, and other rich multimedia functions. It has two display interfaces, RGB/MIPI, and supports a maximum screen resolution of 1920 * 1080. Supports SPI/UART communication with external controllers and multiple UI firmware upgrade modes. Minimalist peripheral circuit requirements, using external memory to minimize user BOM costs. The supporting upper computer can visually configure the chip parameters, easily adapt to different screen parameters and related functions, and is simple and easy to use. Taking the ZDP1440P128D application diagram as an example.

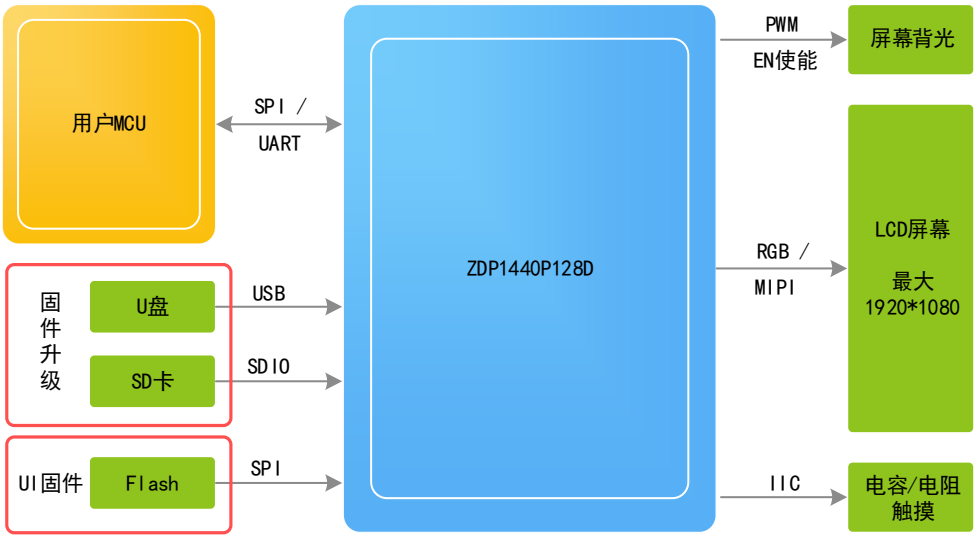


Figure 1.1 ZDP14x0 Functional Block Diagram

1.2 Features

- Built in AWTK GUI engine, paired with AWTK Designer upper computer drag and drop development;
- Built in 64MB/16MB display memory;
- Built in image processing, supports 2D graphics acceleration, rotation, scaling, and supports alpha blend;
- Built in audio decoding, audio playback;
- Support RGB and MIPI interface LCD screens;
- The maximum resolution supports 1920 * 1080;
- Support screen resistance touch and capacitor touch options;
- Supports backlight adjustment and can be equipped with PWM frequency and duty cycle;
- Supporting 1 communication serial port (supporting flow control), SPI slave;
- Support SPI flash interface, NOR and NAND, with configurable capacity;
- Support USB download, USB and SD card upgrades;
- Support 1 channel buzzer interface;
- Status pin, used to check whether the upgrade is successful and whether it is running normally;
- Upgrade enable selection pins, upgrade configuration pins;

- Support configuring the above parameters through the upper computer and downloading them through the burning tool;
- Package: 128-pin ELQFP

1.3 specification

Product	GPU	Memory	working temperature C°	Package	Packing	MPQ	MOQ	MSL
ZDP1440P128D	2D GPU	16MB	-20~+80	LQFP128	TRAY	900	900	3
ZDP1460P128D	2D GPU	64MB	-20~+80	LQFP128	TRAY	900	900	3

2. Signals and Connections

2.1 Pin Definitions

This chip is available in LQFP128 package，The functions of ZDP1440 and ZDP1460 pins are completely identical.。

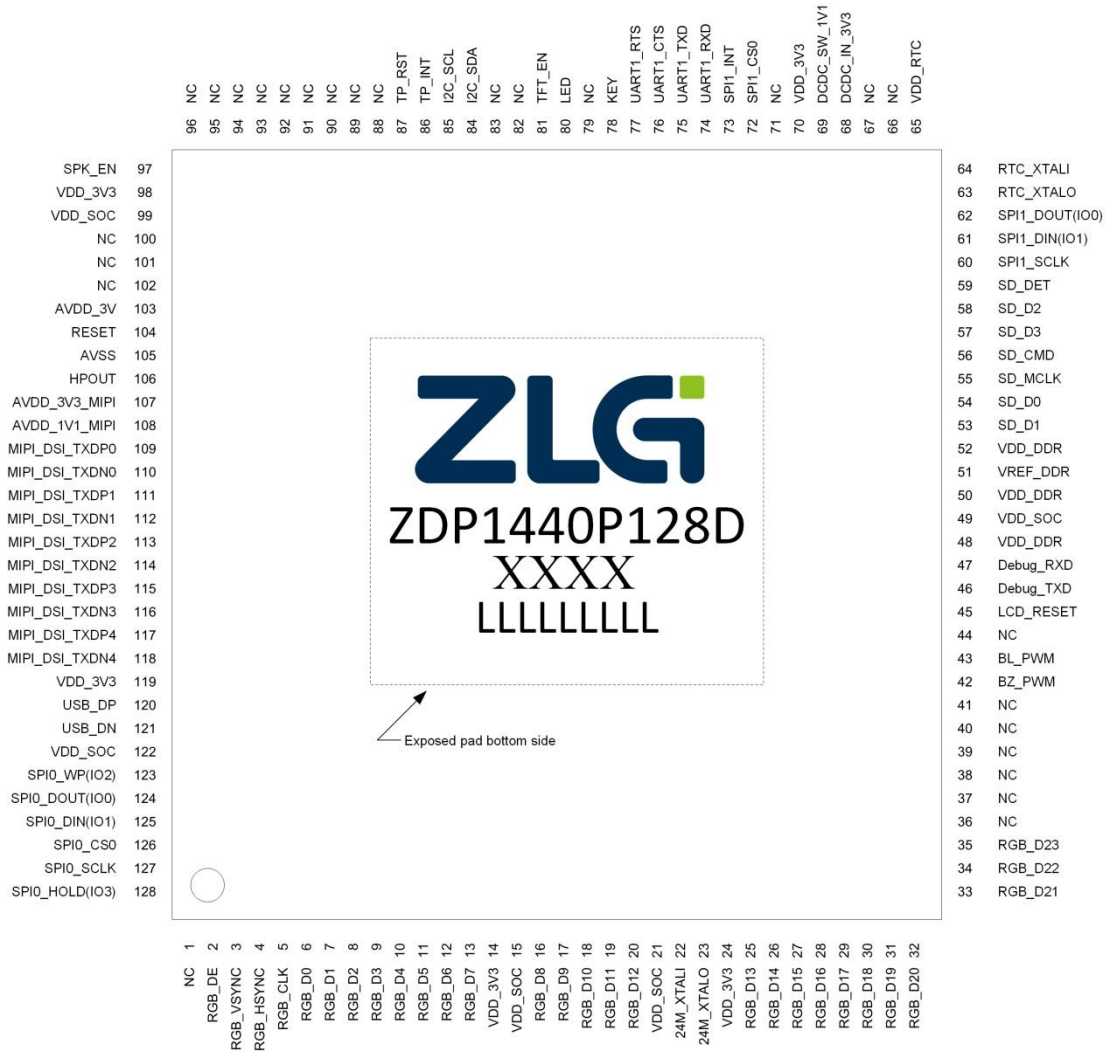


Figure 2.1 ZDP14x0 pin assignment

Fourteen power domains are provided for I/O application, detail definitions are as follows:

- VDD3V3: Universal 3.3V power supply;
- AVDD3V3-MIPI: Provide 3.3V power supply to MIPI;
- AVDD_1V1-MIPI: Provide 1.1V power supply to MIPI;
- VDD0DDR: Provide 1.8V power supply to DDR;
- VDD0RTC: Provides 3.3V power supply to the real-time clock;
- VDD0SOC: Provides 1.1V power supply to the kernel

note：I: input; O: output; IO: input/output; PWR: power supply; GND: ground; A: analog; D: digital. PU: pull-up; PD: pull-down.

Table 2.1 Functional pin Definitions

PIN	PIN NAME	TYPE	Power Domain	RESET	DESCRIPTION
1	NC	-	-	-	free
2	RGB_DE	IO/D	VDD_3V3	I/PU	RGB LCD panel video output effective pixels
3	RGB_VSYNC	IO/D	VDD_3V3	I/PU	Vertical synchronization pulse of RGB LCD video output
4	RGB_HSYNC	IO/D	VDD_3V3	I/PU	Video output horizontal synchronization pulse to RGB LCD
5	RGB_CLK	IO/D	VDD_3V3	I/PU	RGB LCD panel pixel clock signal
6	RGB_D0	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
7	RGB_D1	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
8	RGB_D2	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
9	RGB_D3	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
10	RGB_D4	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
11	RGB_D5	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
12	RGB_D6	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
13	RGB_D7	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
14	VDD_3V3	PWR	VDD_3V3	-	Universal 3.3V power supply
15	VDD_SOC	PWR	VDD_SOC	-	Core power supply
16	RGB_D8	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
17	RGB_D9	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
18	RGB_D10	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
19	RGB_D11	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
20	RGB_D12	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
21	VDD_SOC	PWR	VDD_SOC	-	Core power supply
22	24M_XTALI	I/D	VDD_3V3	-	External 24MHz crystal oscillator input
23	24M_XTALO	O/D	VDD_3V3	-	External 24MHz crystal oscillator output
24	VDD_3V3	PWR	VDD_3V3	-	Universal 3.3V power supply
25	RGB_D13	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output

PIN	PIN NAME	TYPE	Power Domain	RESET	DESCRIPTION
26	RGB_D14	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
27	RGB_D15	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
28	RGB_D16	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
29	RGB_D17	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
30	RGB_D18	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
31	RGB_D19	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
32	RGB_D20	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
33	RGB_D21	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
34	RGB_D22	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
35	RGB_D23	IO/D	VDD_3V3	I/PU	RGB LCD panel video data output
36	NC	-	-	-	free
37	NC	-	-	-	free
38	NC	-	-	-	free
39	NC	-	-	-	free
40	NC	-	-	-	free
41	NC	-	-	-	free
42	BZ_PWM	IO/D	VDD_3V3	I/PU	Buzzer PWM signal
43	BL_PWM	IO/D	VDD_3V3	I/PD	Backlight PWM signal
44	NC	-	-	-	Free
45	LCD_RESET	IO/D	VDD_3V3	I/PD	LCD panel reset signal
46	Debug _TXD	IO/D	VDD_3V3	I/PU	Debug_tx send data pin
47	Debug _RXD	IO/D	VDD_3V3	I/PU	Debug_rx receive data pin
48	VDD_DDR	PWR	VDD_DDR	-	DDR power supply
49	VDD_SOC	PWR	VDD	-	Core power supply
50	VDD_DDR	PWR	VDD_DDR	-	DDR power supply
51	VREF_DDR	PWR	VREF_DDR	-	DDR reference power input
52	VDD_DDR	PWR	VDD_DDR	-	DDR power supply
53	SD_D1	IO/D	VDD_3V3	I/PU	SD data cable
54	SD_D0	IO/D	VDD_3V3	I/PU	SD data cable
55	SD_MCLK	IO/D	VDD_3V3	I/PD	SD Master Clock
56	SD_CMD	IO/D	VDD_3V3	I/PU	SD control line

PIN	PIN NAME	TYPE	Power Domain	RESET	DESCRIPTION
57	SD_D3	IO/D	VDD_3V3	I/PU	SD data cable
58	SD_D2	IO/D	VDD_3V3	I/PU	SD data cable
59	SD_DET	IO/D	VDD_3V3	I/PU	SD card insertion detection
60	SPI1_SCLK	IO/D	VDD_3V3	I/PU	SPI1 clock
61	SPI1_DIN(IO1)	IO/D	VDD_3V3	I/PU	SPI1 data input (serial data input/output 1)
62	SPI1_DOUT(IO0)	IO/D	VDD_3V3	I/PU	SPI1 data output (serial data input/output 0)
63	RTC_XTALO	O/D	VDD_3V3	-	External 32.768KHz crystal oscillator output
64	RTC_XTALI	I/D	VDD_3V3	-	External 32.768KHz crystal oscillator input
65	VDD_RTC	PWR	VDD_RTC	-	Battery voltage input pin, providing power for RTC and PMU
66	NC	-	-	-	Free
67	NC	-	-	-	Free
68	DCDC_IN_3V3	PWR	DCDC_IN_3V3	-	Internal PMU power input pin
69	DCDC_SW_1V1	O/A	DCDC_IN_3V3	-	DCDC output switch pin
70	VDD_3V3	PWR	VDD_3V3	-	Universal 3.3V power supply
71	NC	-	-	-	Free
72	SPI1_CS0	IO/D	VDD_3V3	I/PU	SPI1 film selection 0
73	SPI1_INT	IO/D	VDD_3V3	I/PU	SPI1 interrupt receive signal
74	UART1_RXD	IO/D	VDD_3V3	I/PU	UART1 receiving pin
75	UART1_TXD	IO/D	VDD_3V3	I/PU	UART1 send pin
76	UART1_CTS	IO/D	VDD_3V3	I/PU	UART1 clear transmission signal
77	UART1_RTS	IO/D	VDD_3V3	I/PU	Signal ready to be sent by UART1
78	KEY	IO/D	VDD_3V3	I/PU	Upgrade button pins
79	NC	-	-	-	Free
80	LED	IO/D	VDD_3V3	I/PU	LED pins
81	TFT_EN	IO/D	VDD_3V3	I/PU	TFT LCD screen enable pin
82	NC	-	-	-	Free

PIN	PIN NAME	TYPE	Power Domain	RESET	DESCRIPTION
83	NC	-	-	-	Free
84	I2C_SDA	IO/D	VDD_3V3	I/PU	Touch I2C serial data
85	I2C_SCL	IO/D	VDD_3V3	I/PU	Touch I2C serial clock
86	TP_INT	IO/D	VDD_3V3	I/PU	Touch screen interrupt pin
87	TP_RST	IO/D	VDD_3V3	I/PU	Touch screen reset pin
88	NC	-	-	-	free
89	NC	-	-	-	free
90	NC	-	-	-	free
91	NC	-	-	-	free
92	NC	-	-	-	free
93	NC	-	-	-	free
94	NC	-	-	-	free
95	NC	-	-	-	free
96	NC	-	-	-	free
97	SPK_EN	IO/D	VDD_3V3	I/PU	Audio amplifier enable control pin
98	VDD_3V3	PWR	VDD_3V3	-	Universal 3.3V power supply
99	VDD_SOC	PWR	VDD_SOC	-	Core power supply
100	NC	-	-	-	Free
101	NC	-	-	-	Free
102	NC	-	-	-	Free
103	AVDD_3V	O/A	AVDD_3V3_MIPI	-	Third reference voltage (3.0V). To filter out noise, it is recommended to connect a 4.7 between this pin and GND μ F or 10 μ F and a 0.1 μ F capacitor.
104	RESET	O/A	AVDD_3V3_MIPI	-	Power on reset pin, effective at high level
105	AVSS	GND/A	-	-	The reference site needs to be kept clean and low noise
106	HPOUT	O/A	HPVDD	-	Audio output pin
107	AVDD_3V3_MIPI	PWR	AVDD_3V3_MIPI	-	MIPI LCD power pin
108	AVDD_1V1_MIPI	O/PWR	AVDD_1V1_MIPI	-	MIPI LCD power pin
109	MIPI_DSI_TXDP0	A	AVDD_3V3_MIPI	-	MIPI DSI lane 0 (+)
110	MIPI_DSI_TXDN0	A	AVDD_3V3_MIPI	-	MIPI DSI lane 0 (-)
111	MIPI_DSI_TXDP1	A	AVDD_3V3_MIPI	-	MIPI DSI lane 1(+)

PIN	PIN NAME	TYPE	Power Domain	RESET	DESCRIPTION
112	MIPI_DSI_TXDN1	A	AVDD_3V3_MIPI	-	MIPI DSI lane 1 (-)
113	MIPI_DSI_TXDP2	A	AVDD_3V3_MIPI	-	MIPI DSI lane 2 (+)
114	MIPI_DSI_TXDN2	A	AVDD_3V3_MIPI	-	MIPI DSI lane 2 (-)
115	MIPI_DSI_TXDP3	A	AVDD_3V3_MIPI	-	MIPI DSI lane 3(+)
116	MIPI_DSI_TXDN3	A	AVDD_3V3_MIPI	-	MIPI DSI lane 3 (-)
117	MIPI_DSI_TXDP4	A	AVDD_3V3_MIPI	-	MIPI DSI lane 4(+)
118	MIPI_DSI_TXDN4	A	AVDD_3V3_MIPI	-	MIPI DSI lane 4 (-)
119	VDD_3V3	PWR	VDD_3V3	-	Universal 3.3V power supply
120	USB_DP	A	VDD_3V3	-	USB data positive pin (D+)
121	USB_DN	A	VDD_3V3	-	USB data negative pin (D -)
122	VDD_SOC	PWR	VDD_SOC	-	Core power supply
123	SPI0_WP(IO2)	IO/D	VDD_3V3	I/PU	SPI0 read protection (serial input/output 2)
124	SPI0_DOUT(IO0)	IO/D	VDD_3V3	I/PU	SPI0 data output (serial input/output 0)
125	SPI0_DIN(IO1)	IO/D	VDD_3V3	I/PU	SPI0 data input (serial input/output 1)
126	SPI0_CS0	IO/D	VDD_3V3	I/PU	SPI0 film selection 0
127	SPI0_SCLK	IO/D	VDD_3V3	I/PU	SPI0 clock
128	SPI0_HOLD(IO3)	IO/D	VDD_3V3	I/PU	SPI0 HOLD (serial input/output 3)
129	GND	GND	-	-	Universally, the power ground that connects the entire chip circuit

3. Electrical Specifications

3.1 Maximum Ratings

This part aims to list the recommended stress ratings, and stresses greater than those listed may cause permanent damage to the device. Functional operations of the device at these or any other conditions outside those indicted in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

Table 3.1 ZDP14x0 Maximum Ratings

RATING	SYMBOL	MIN.	MAX.	UNIT
VDD0SOC voltage relative to e-GND	VDD_SOC	-0.30	1.40	V
Voltage of VDD3V3 relative to e-GND	VDD_3V3	-0.30	4.00	V
AVDD3V3-MIPI voltage relative to e-GND	AVDD_3V3_MIPI	-0.30	4.00	V
AVDD_1V1-MIPI voltage relative to e-GND	AVDD_1V1_MIPI	-0.30	1.40	V
VDD0DDR voltage relative to e-GND	VDD_DDR	-0.30	2.30	V
VDD0RTC voltage relative to e-GND	VDD_RTC	-0.30	4.00	V
Voltage of DCDC-IN3V3 relative to e-GND	DCDC_IN_3V3	3.30	3.75	V
Operating Temperature Range note 1	Ta	-20	80	V
Storage Temperature	Ts	-	125	℃
Electrostatic Discharge Voltage (Human-body Mode)	$V_{ESD(HBM)}$	-	±2.00	KV

NOTE：

1. Operating Temperature Range in the above table refers to ambient temperature range.
2. ESD HBM test is based on MIL-STD-883G Method 3015.7.

3.2 Recommended Operating Range

Table 3.2 Recommended Operating Range

RATING	SYMBOL	MIN.	MAX.	UNIT
VDD0SOC voltage relative to e-GND	VDD_SOC	-0.30	1.10	1.40
Voltage of VDD3V3 relative to e-GND	VDD_3V3	-0.30	3.30	4.00
AVDD3V3-MIPI voltage relative to e-GND	AVDD_3V3_MIPI	-0.30	3.30	4.00
AVDD_1V1-MIPI voltage relative to e-GND	AVDD_1V1_MIPI	-0.30	1.20	1.40
VDD0DDR voltage relative to e-GND	VDD_DDR	-0.30	1.80	2.30
VDD0RTC voltage relative to e-GND	VDD_RTC	-0.30	3.30	4.00
Voltage of DCDC-IN3V3 relative to e-GND	DCDC_IN_3V3	3.30	3.50	3.75

3.3 Electrical Characteristics of PMU

Typical values are at TA = +27°C VBAT=3.70 and all Current Values are dynamic, unless other-

wise noted.

Table 3.3 Electrical Characteristics of BUCK11

RATING	SYMBOL	CONDITION	TYP.	UNIT
Operating supply voltage	Vin	ILOAD_max=350mA	3.30-3.75	V
Output voltage	Vout	0mA<ILOAD<350mA	0.85-1.30	V
Output voltage	Vout(accuracy)	27 ℃	+/-3	%
MAX Output current	ILOAD_MAX	3.30V<VIN<4.20V	350	mA
Vin Quiescent Current	INO_LOAD	ILOAD=0mA	<100	μA
Vin Shutdown Current	Ipowerdown	27 ℃	<1	μA
Output Voltage Ripple	Vripple	ILOAD=100mA,ESR< 4 0mΩ	<40	mV
Efficiency	η	ILOAD=100mA	83	%
OSC Frequency	OSC Frequency	27 ℃	1000	KHz
Peak Current Limit	Limit	27 ℃	750	mA
P-Channel On-Resistance	Rpswitch	VIN=3.50V	500	mΩ

3.4 DC Electrical Characteristics

Table 3.4 DC Electrical Characteristics (3.3V IO Application)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage	VIH	2.00	-	VDDIO+0.30	V
Input Low Voltage	VIL	-0.30	-	0.80	V
Output High Voltage @ IOH(min)	VOH	2.40	-	-	V
Output Low Voltage @IOL (min)	VOL	-	-	0.40	V
Input Leakage Current	IL	-	-	±10	μA
Tri-state Output Leakage Current	IOZ	-	-	±10	μA
Headphone output load resistance	RHP	-	32	-	Ω

NOTE：IOL and IOH condition should refer to the particular value according to the different driving strength.

Table 3.5 DC Electrical Characteristics (1.8V IO Application)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage	VIH	0.65*VDDIO	-	VDDIO+0.30	V
Input Low Voltage	VIL	-0.30	-	0.35*VDDIO	V
Output High Voltage @ IOH(min)	VOH	VDDIO-0.45	-	-	V
Output Low Voltage@ IOL (min)	VOL	-	-	0.45	V
Input Leakage Current	IL	-	-	±10	μA
Tri-state Output Leakage Current	IOZ	-	-	±10	μA
Headphone output load resistance	RHP	-	32	-	Ω

3.5 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency ranging from 0 MHz to 340 MHz.

Table 3.6 32K/24M Oscillator Signal Timing

PARAMETER	MIN.	TYP.	MAX.	UNIT
XTAL32K Startup Time	-	-	1.30	s
XTAL24M Startup Time	-	6	-	ms

Table 3.7 HS Receiver AC specifications (only for MIPI CSI mode)

PARAMETER	MIN.	TYP.	MAX.	UNIT
△VCMRX(HF)	-	-	0.10	V

△VCMRX(LF)	-0.05	-	0.05	V

NOTE：

1) Excluding “static” ground shift of 50mV.
2) VCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
3) For higher bit rates a 14 pF capacitor will be needed to meet the common-mode return loss specification.
4) Voltage difference compared to the DC average common mode potential

Table 3.8 LP Receiver AC specifications (only for MIPI CSI mode)

PARAMETER	MIN.	TYP.	MAX.	UNIT
ESPIKE	-	-	0.30	V
TMINRX	20	-	-	ns
VINT	-	-	0.20	V
FINT	450	-	-	MHz

NOTE：

1. Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state.
2. An impulse less than this will not change the receiver state.
3. In addition to the required glitch rejection, implementer shall ensure rejection of known RF-interferers.
4. An input pulse greater than this shall toggle the output.

Table 3.9 CMOS Receiver AC specifications (CMOS mode)

PARAMETER	MIN.	TYP.	MAX.	UNIT
TMIN-RX	8	-	-	ns
VINT	-	-	0.20	V
FINT	450	-	-	MHz

4. Typical application circuits

The following circuits are typical design applications for the smallest system and some peripherals. For peripheral circuits that are not recommended, please design them according to relevant manuals.

4.1 Power

It is recommended to configure at least one decoupling capacitor for each power pin of the chip. When wiring, the decoupling capacitor should be placed as close as possible to the pins, and the power supply should first pass through the decoupling capacitor before reaching the chip pins. The power pins and corresponding voltage range of the chip are shown in table 4.1。

table 4.1 Chip Power Pin Description

Number	name	explain	Voltage range（V）	TYP	Importance level
1	VDD_SOC	Chip core power supply	1.00~1.25	input	must
3	VDD_DDR	Memory power supply	1.70~1.90	input	must
4	VREF_DDR	Memory reference voltage	VDD_DDR	input	must
5	VDD_3V3	Universal IO power supply	2.97~3.63	input	must
7	AVDD_3V	Audio analog power supply	3.00	output	must
9	VDD_RTC	RTC power supply	2.97~3.63	input	must
11	AVDD_3V3_MIPI	MIPI displays PHY power supply	2.97~3.63	input	must
12	AVDD_1V1_MIPI	MIPI display PHY power supply	1.14~1.26	output	Optional

Note: AVDD_1V and AVDD_1V1-MIPI are output power supplies, and decoupling capacitors should be connected externally. The recommended capacitance value is 4.7 μ F and 0.1 μ F. Placing pins close to the chip; VDD3V3 is a universal 3.3V input power supply, and it is recommended to have at least one 0.1 per power pin μ F capacitor, with at least one 4.7 configured on two power pins μ F capacitor.

4.2 PMU

4.2.1 PMU internal structure

The integrated PMU module inside the chip mainly supplies power to CORE, and the corresponding output is DCDC_SW_1V1. As shown in Figure 4.1, the feedback circuit pin of DCDC_SW_1V1 is integrated into the input pin of VDD0SOC.

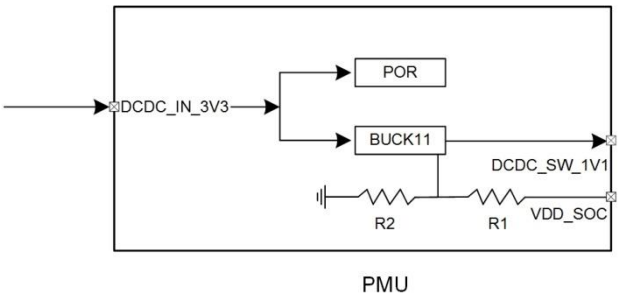


Figure 4.2 integrated PMU module

NOTE：

1. The PMU module integrates a monitoring circuit internally, supporting chip power-off reset and power-on reset release. The specific threshold values are divided into three levels: 2.55V, 2.65V (default), and 2.75V;
2. Whether to use internal PMU 1.1V output, please refer to the schematic design.

4.2.2 PMU

DCDC-IN3V3 is the power input pin of the chip PMU. When designing the circuit, a set of filtering capacitors (recommended combination is 22uF and 100nF) should be placed at the DCDC-IN3V3 pin. As shown in Figure 4.3 .

The output of the PMU module of the chip's DCDC-SW_1V1 (output range [0.9V~1.3V]) needs to be combined with external inductive and capacitive devices to form a step-down circuit. It is recommended to use a combination of inductance 4.7uH and capacitors 22uF and 100nF.

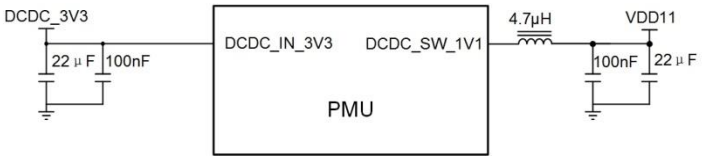


Figure 4.3 PMU Reference circuit

NOTE: The input wiring of VIN needs to be at least 12mil, and the capacitor should be as close as possible to the chip pins; Inductors and capacitors should be placed adjacent to the chip pins, with a wiring width of more than 12 mils; The FB pin of the BUCK circuit is located on the VDD0SOC pin of the chip, ensuring that the current circuit is sufficiently short.

4.2.3 Voltage Range Parameters

table 4.2shows the voltage range parameters of the PMU module of the chip.

table 4.2 PMU Range Parameters

num	Name	Function Description	Input voltage range（V）			Output voltage range（V）			Output current（mA）
			MIN	TYP	MAX	MIN	TYP	MAX	Avg
1	DCDC_IN_3V3	Input power supply	3.13	3.30	3.63	-	-	-	-
2	DCDC_SW_1V1	Output power supply	-	-	-	0.9	1.25	1.3	350

4.3 System module power pins

4.3.1 VDD_DDR 和 VREF_DDR

The VDD0DDR/VREF-DDR pins provide power to the memory of the chip. The pins of VDD0DR are concentrated, making it difficult to ensure that each pin is equipped with a decoupling capacitor during wiring. Therefore, adjacent pins can use the same decoupling capacitor.

VREF-DDR can use a resistive voltage divider circuit, as shown in Figure 4.4.

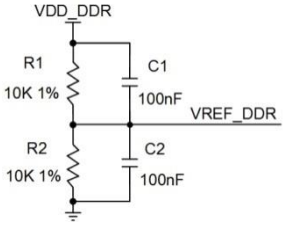


Figure 4.4 VREF-DDR power supply circuit

Please note:
1. The resistance accuracy at R1 and R2 should be ≤ 1%;
When PCB layout, C1, C2, R1, and R2 need to be close to the chip pins;
3. DDR needs to ensure a stable power supply of at least 1.7V~1.9V.

4.4 Clock

The chip has two clock generation circuits: a 32.768KHz clock generation circuit and a 24MHz clock generation circuit.

1. The 32.768KHz clock generation circuit generates a synchronous clock signal for real-time clock (RTC), supporting real-time clock timing and perpetual calendar calculation functions;

The 24MHz clock generation circuit generates the chip's working clock.

When selecting crystal oscillators, attention should be paid to:

The frequency error of 24MHz crystal oscillator and 32.768KHz crystal oscillator shall not exceed ± 20ppm;

2. The chip has integrated a 24MHz crystal oscillator load capacitor inside, so there is no need for external capacitors and only the position can be reserved.

4.4.1 24MHz crystal oscillator circuit

24MHz crystal oscillator circuit (crystal oscillator load capacitance CL=10pF), as shown in Figure 4.5.

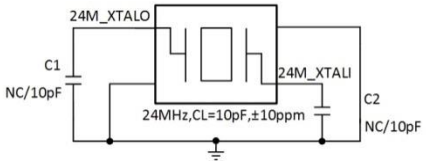


Figure 4.5 24MHz crystal oscillator circuit

When designing, it should be noted that the range of the integrated 24MHz crystal oscillator load capacitor inside the chip is 6pF to 14pF. The external capacitance value needs to be configured according to the actual situation.

4.4.2 32.768KHz 晶振电路

32.768KHz crystal oscillator circuit (crystal oscillator load capacitance CL=12.5pF), reference circuit as shown in Figure 4.6.

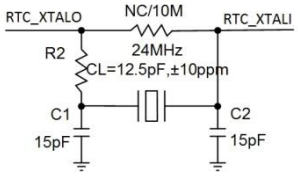


Figure 4.6 32.768KHz crystal oscillator circuit

4.5 RESET

The RESET pin of the chip is the system reset control pin. When the level is raised, it will reset all modules inside the chip except for RTC to a predefined reset state. RESET needs to connect a 4.7uF capacitor to the ground near the chip pin on the circuit, as shown in Figure 4.7.

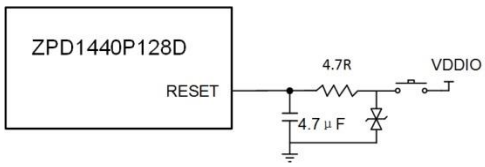


Figure 4.7 ZDP14x0P128D chip reset circuit diagram

4.6 BOOT

When designing chip circuits, it is recommended to pull down the SPI0-DOUT pin by connecting a 100 Ω resistor and a button for program startup debugging.

4.7 SPI flash

The SPI0 interface of the chip is the startup program interface, with NOR/NAND flash external, and a maximum speed of 125MHz. When SPI0 is connected to Flash, it supports one line and four line bidirectional communication modes, as shown in Figure 4.8. It is recommended to use 4-wire mode to further improve the overall communication speed.

Attention:

1. SPI0 is used to connect programs to start Flash, external NOR Flash or NAND Flash.
2. SPI0 supports Flash hardware reset, so SPI0_HOLD needs to be connected to the Flash chip.
3. The docking of the two data lines of the SPI0 interface must comply with the docking relationship between MOSI and MISO.
4. If the clock of SPI application is higher than 25MHz, termination design can be considered to ensure the integrity of SPI signal.

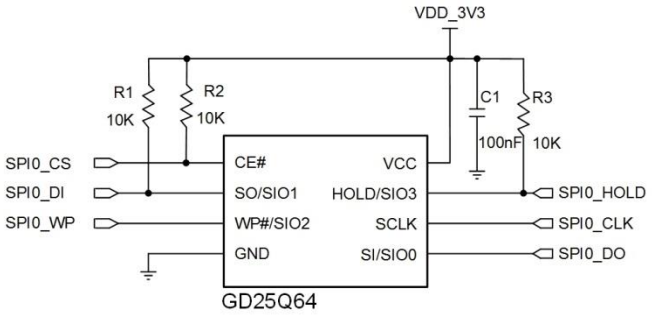


Figure 4.8 SPI Flash Four Wire Mode Circuit Diagram

4.8 USB

The chip supports one USB 2.0 interface and can operate in Device/Host mode. USB is initially used for program downloads (Device function), and after burning factory firmware, it is only used for USB drive upgrades (Host function).

The USB schematic design is relatively simple, just pay attention to the DP and DN line sequence correspondence. Due to the insufficient ESD performance of the chip USB, it is necessary to add ESD protection devices during the design process。

Attention should be paid to the selection of ESD devices:

1. The parasitic capacitance of the ESD device on the USBDN and USBDP signal lines should be less than 3pF.
2. To improve the ESD resistance performance of the USB interface, the terminal housing of the USB can be grounded by configuring a magnetic bead or a small inductor, or a common mode suppression inductor can be connected in series on the USBDN and USBDP signal lines.

4.9 SD card interface

The chip provides an SD interface specifically for external TF (Micro SD) cards, which can be used for UI firmware upgrades.

Attention:

1. When using an SD card to upgrade UI firmware, the SD interface is used for external TF cards, and the SD card upgrade method is not used. The interface is suspended;
2. SD-CMD and SD-D0~D3 should support pull-up function. When designing, attention should be paid to whether external pull-up is supported, otherwise pull-up processing needs to be performed.

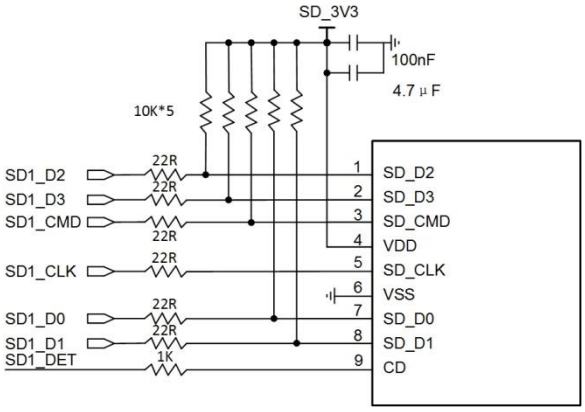


Figure 4.9 SD card reference circuit

4.10 LCD

The chip supports both MIPI/RGB display interfaces.

Attention: When assembling the LCD screen, it is necessary to add conductive cotton to connect the ground of the display screen casing to the ground of the PCB.

4.10.1 MIPI interfaces

The default MIPI clock line uses MIPI-DSI-TXDP2/MIPI-DSI-TXDN2 as the MIPI clock line, as shown in Figure 4.10 .

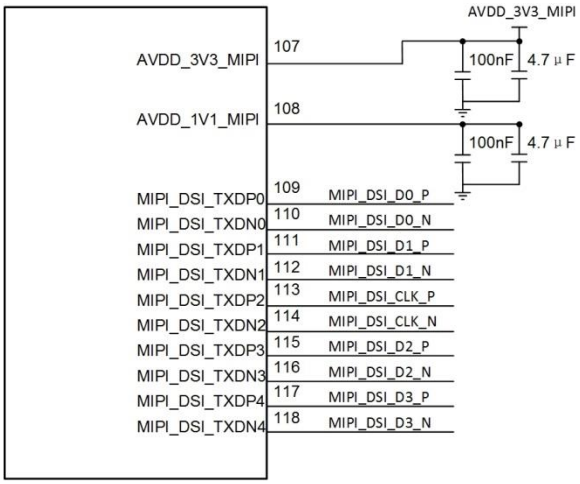


Figure 4.10 MIPI Display Interface Diagram

The power pins of the MIPI display screen include AVDD3V3-MIPI and AVDD_1V1-MIPI. AVDD3V3-MIPI is powered by 3.3V; AVDD_1V1-MIPI is the 1.1V voltage generated internally within the chip, which requires an external capacitor of 1uF or greater.

4.10.2 RGB Interface

1. The RGB interface of the chip has the following characteristics:
2. Supports 16 bit, 18 bit, and 24 bit interfaces;
3. The maximum resolution supported by RGB display screens is 1280 * 800; The frame rate range is [50fps~60fps];

The commonly used data formats for 16 bit/18 bit/24 bit RGB displays include RGB565, BGR565, RGB666, BGR666, RGB888 (default chip value), and BGR888. The interface sequence of RGB display screens: R is the high bit, G is the middle bit, B is the low bit, and other formats are shown in

4. table 4.3.

table 4.3 Order of RGB interfaces in different scenarios

Application scenarios	The interface sequence of RGB display screens
16 bit RGB display screen (i.e. line sequence of RGB565)	DATA[23:19] = R[4:0]； DATA[15:10]= G[5:0] DATA[7:3] = B[4:0]
18 bit RGB display screen (i.e. the line sequence of RGB666)	DATA[23:18] = R[5:0]； DATA[15:10] = G[5:0]； DATA[7:2] = B[5:0]
24 bit RGB display screen (i.e. the line sequence of RGB888)	DATA[23:16] = R[7:0]； DATA[15:8] = G[7:0]； DATA[7:0] = B[7:0]
A 24 bit RGB display screen (i.e. the line sequence of RGB888), using only RGB565, with other data cables connected in an empty space	DATA[23:19] = R[7:3]； DATA[15:10]= G[7:2] DATA[7:3] = B[7:3]

4.11 Communication Interface

The chip supports communication with other devices through UART or SPI, and defaults to using UART1 to communicate with other devices.

- The chip supports 2 serial ports, among which UART0 is the default debugging serial port used for printing debugging information. Users can debug code based on the printed information;
- UART1 is used for communication between users and other devices, and supports optional flow control (parameter configuration on the upper computer);
- The SPI1 of the chip is a regular SPI interface, which can be used for slave communication with devices (using either UART1 or UART1), and it needs to be correctly connected during design.

4.12 Touch interface

The chip supports one I2C interface, which is used for resistive screen AD acquisition chips or capacitive screen touch chips. Please note:

1. Resistance touch, default external XPT7603;
2. Capacitive touch, default external GT911;
3. The pull-up resistance of peripheral hardware is 4.7K Ω to 10K Ω;
4. Other types of touch chips can be selected based on parameter configuration on the upper computer. If the touch chip model used is not supported, you can contact the original factory to add it.

4.13 Others

In addition to the above functions, the chip also supports the following specific functions, which can be directly configured by the upper computer:

1. The chip supports a dedicated audio output interface HPOUT pin, with the addition of an audio chip. The upper computer is configured to enable audio;
2. The chip supports backlight enable and brightness adjustment, and the upper computer supports brightness configuration;
3. The chip supports active and passive buzzer drivers, and the upper computer supports configuring the driver duty cycle;
4. The chip supports one status prompt pin, which can be used for LED status prompts;
5. The chip supports a key input key for upgrading and enabling.

5. Package Information

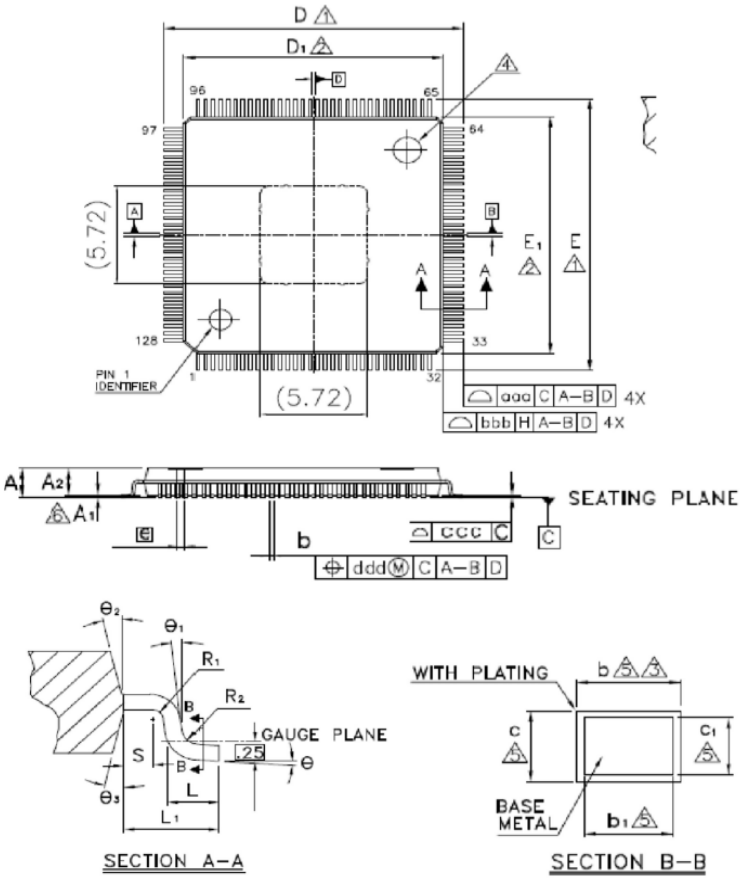


Figure 5.1 ZDP14x0 package

Table 5.1 Dimension parameters

SYMBOL	Dimension in mm		
	MIN	NOM	MAX
A	-	-	1.6
A1	0.025	-	0.127
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
c	0.09	0.14	0.20
c1	0.09	0.12	0.16
D	15.85	16.00	16.15
D1	13.90	14.00	14.10
E	15.85	16.00	16.15
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	-	-

SYMBOL	Dimension in mm		
	MIN	NOM	MAX
R2	0.08	-	0.20
S	0.20	-	-
θ	0 °	3.5 °	7 °
θ1	0 °	-	-
θ2	11 °	12 °	13 °
θ3	11 °	12 °	13 °
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.07		

6. Reflow Profile

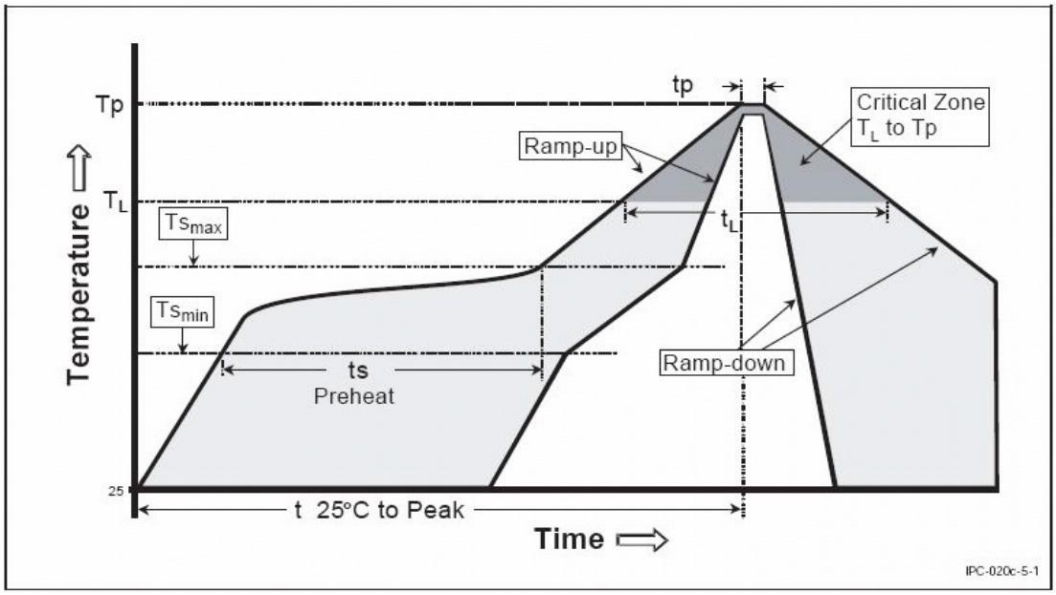


Figure 6.1 Recommended Reflow Profile

Profile Feature	Pb-Free Assembly
Average ramp-up rate (Tsmax to TP)	2 ℃/second max
Preheat -Temperature Min(Tsmin) -Temperature Max(Tsmax) -Time (minto max) (ts)	150 ℃ 200 ℃ 60 – 180 seconds
Time maintained above: -Temperature (TL) -Time (tL)	60 – 150 seconds
Peak Temperature (TP)	260 ℃
Time within 5℃ of actual Peak Temperature(tp)	30 seconds max
Ramp-down Rate	3℃/second max
Time 25℃ to Peak Temperature	8 minutes max

Note: All temperatures refer to topside of the package, measured on the package body surface.

7. Storage and Baking

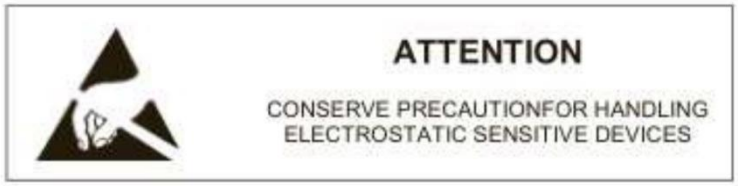
1. Package moisture sensitivity is level 3.
2. Shelf life in sealed bag: 12 months at < 30℃ and < 60% relative humidity (RH).
3. After bag is opened, device that will be subjected to reflow solder or other high temperature process must be:

- Mounted within: 168 hours of factory conditions < 30℃/60% RH or
- Stored at < 20% RH.

4. Devices require bake, before mounting, if:

- Humidity indicator card reads = 20% when read at 25 ± 5℃;
- 2a or 2bare not met.

5. If baking is required, device maybe baked for 12 hours at 125℃± 5℃.



6. 图 7.1 ATTENTION

8. Disclaimer

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